N-63-4-3

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# THIRD QUARTERLY REPORT

# PRODUCTION ENGINEERING MEASURE

## PRODUCTION DEVELOPMENT

## OF A

## SILICON PLANAR EPITAXIAL TRANSISTOR

Report Period:

NOVEMBER 1, 1962 TO JANUARY 31, 1963

CONTRACT NO: DA-36-039-SC86728

Placed By

U.S. ARMY ELECTRONICS MATERIEL AGENCY

PHILADELPHIA 3, PENNSYLVANIA

410097

FROM DIODES TO INTEGRATED CIRCUITS...
ADVANCED TECHNOLOGY THROUGH MOTOROLA RESEARCH

THIRD QUARTERLY REPORT

PRODUCTION ENGINEERING MEASURE

# "PRODUCTION DEVELOPMENT OF A SILICON PLANAR EPITAXIAL TRANSISTOR WITH A MAXIMUM OPERATING FAILURE RATE OF 0.001% PER 1000 HOURS AT A CONFIDENCE LEVEL OF 90% AT 25°C"

ORDER NO. 19050-PP-62-81-81

CONTRACT NO. DA-36-039-SC86728

THIS REPORT COVERS THE CONTRACT PERIOD:

NOVEMBER 1, 1962 TO JANUARY 31, 1963

SUBMITTED BY:

MOTOROLA, INC.

SEMICONDUCTOR PRODUCTS DIVISION

5005 E. McDOWELL RD.

PHOENIX 8, ARIZONA

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## 1.0 PURPOSE OF CONTRACT

The purpose of this contract is to improve production techniques in order to increase the reliability of Silicon Planar Epitaxial Transistor Type 2N696 with a maximum operating failure rate of 0.001% per 1000 hours at a confidence level of 90% at 25°C as an objective. The failure rate is an objective, and as a minimum all of the following Manufacturing processes are to be improved toward attaining or exceeding the specified failure rate:

a. Surface Preparation
b. Diffusion Processing
c. Epitaxial Starting Material
d. Wire Bonding
e. Metallizing
f. Geometry Definition.

In addition, this report outlines the Engineering and Reliability progress made during the reporting period.

## 2.0 ABSTRACT

No changes were made in the Surface Preparation and Epitaxial Starting Material processes during this reporting period. However, work was done on the Die Bonding and Welding processes during the reporting period, and these improvements are reported on.

The most significant changes involve a switch from gold to aluminum metalization.

Another major process improvement involves the conversion of the base diffusion from boron oxide to a boron trichloride process.

## 3.0 MANUFACTURING PROCESSES TO BE IMPROVED

### 3.1 Epitaxial Starting Material

No changes were made in this process during the reporting period.

### 3.2 Surface Preparation

No changes were made in this process during the reporting period.

## 3.3 Geometry Definition (Tom Kearkuff)

### 3.3.1 KMER

New KMER hoods are being evaluated which employ an air curtain over the front of the hood. Measurements indicate that these hoods will show a great improvement in dust count over present "clean" rooms. The filtered air is recirculated ensuring maximum efficiency of the filter. The incidence of pin holes and other KMER defects is considerably reduced in thse hoods.

## 3.4 Metalization (Mike Cassidy)

The gold system, despite it's advantage in monometallic construction, has several disadvantages:

a. Deterioration of low current beta with decreasing temperature.
b. Rapidly increasing $V_{be}$ with decreasing temperature.
c. Necessity for an extremely good atmosphere in the welders. Rapid deterioration occurs if the can is punctured.

For these reasons, and also to improve processing and final test yields, the change was made to aluminum metalization.

Figures 1 and 2 show a comparison of normalized $h_{fe}$ and $V_{BE(SAT)}$ respectively as functions of temperature.

Aluminum units have withstood several thousand hours aging at 300° C with the cans punctured without showing any significant change in electrical parameters.

## 3.5 Wire Bonding (Mike Cassidy)

The switch to aluminum metalization necessitated the development of processes to make adequate contact between the aluminum metalization and the header post. Gold wire was used but this rapidly gave rise to "purple plague", and subsequent mechanical failure under 300° C aging. Aluminum wire with 1% silicon was next evaluated, and by judicious choice

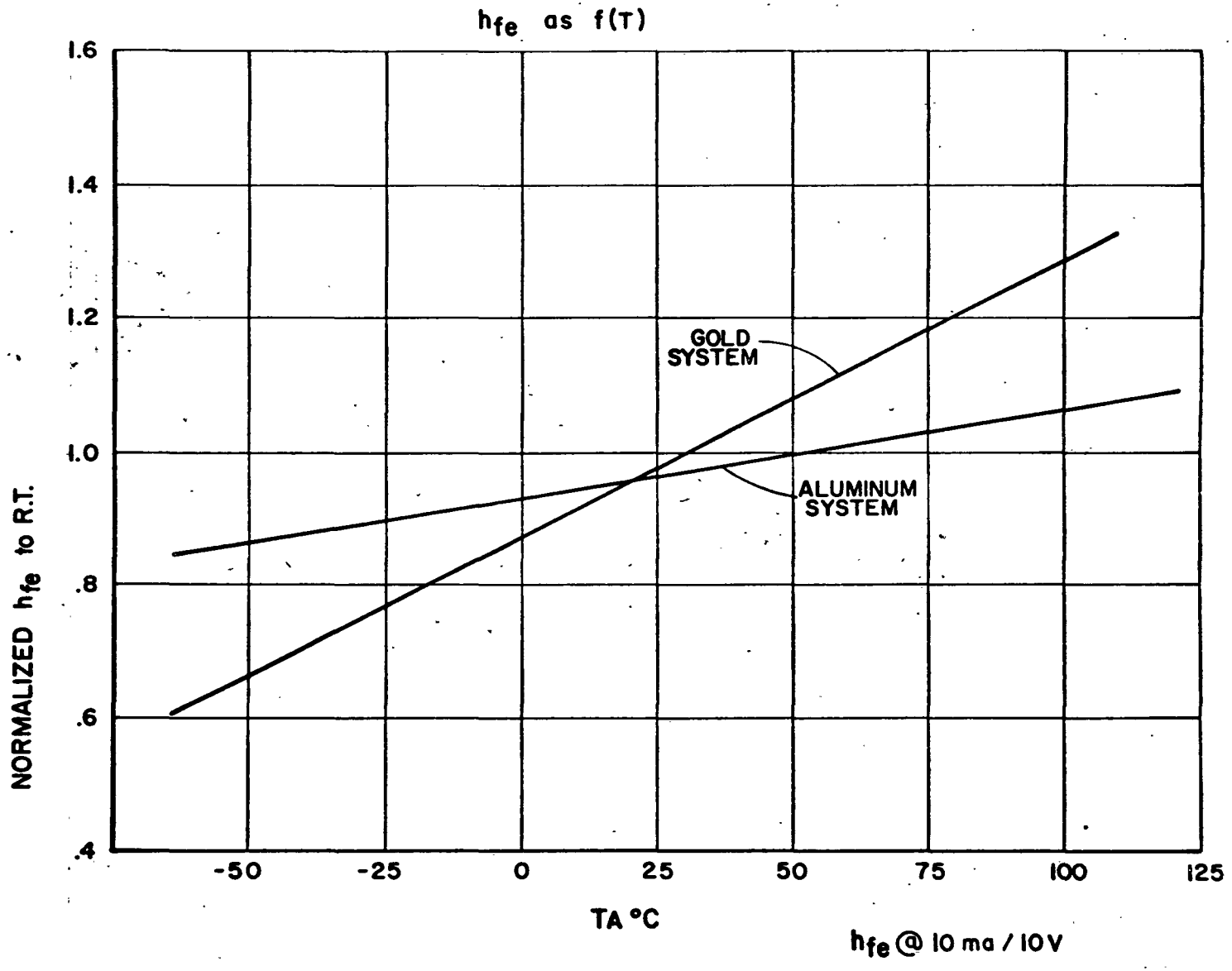

$h_{fe}$ as f(T)
1.6
1.4
1.2
1.0
.8
.6
.4
NORMALIZED $h_{fe}$ to R.T.
GOLD SYSTEM
ALUMINUM SYSTEM
-50
-25
0
25
50
75
100
125
TA °C
$h_{fe}$ @ 10 ma / 10V

FIGURE 1

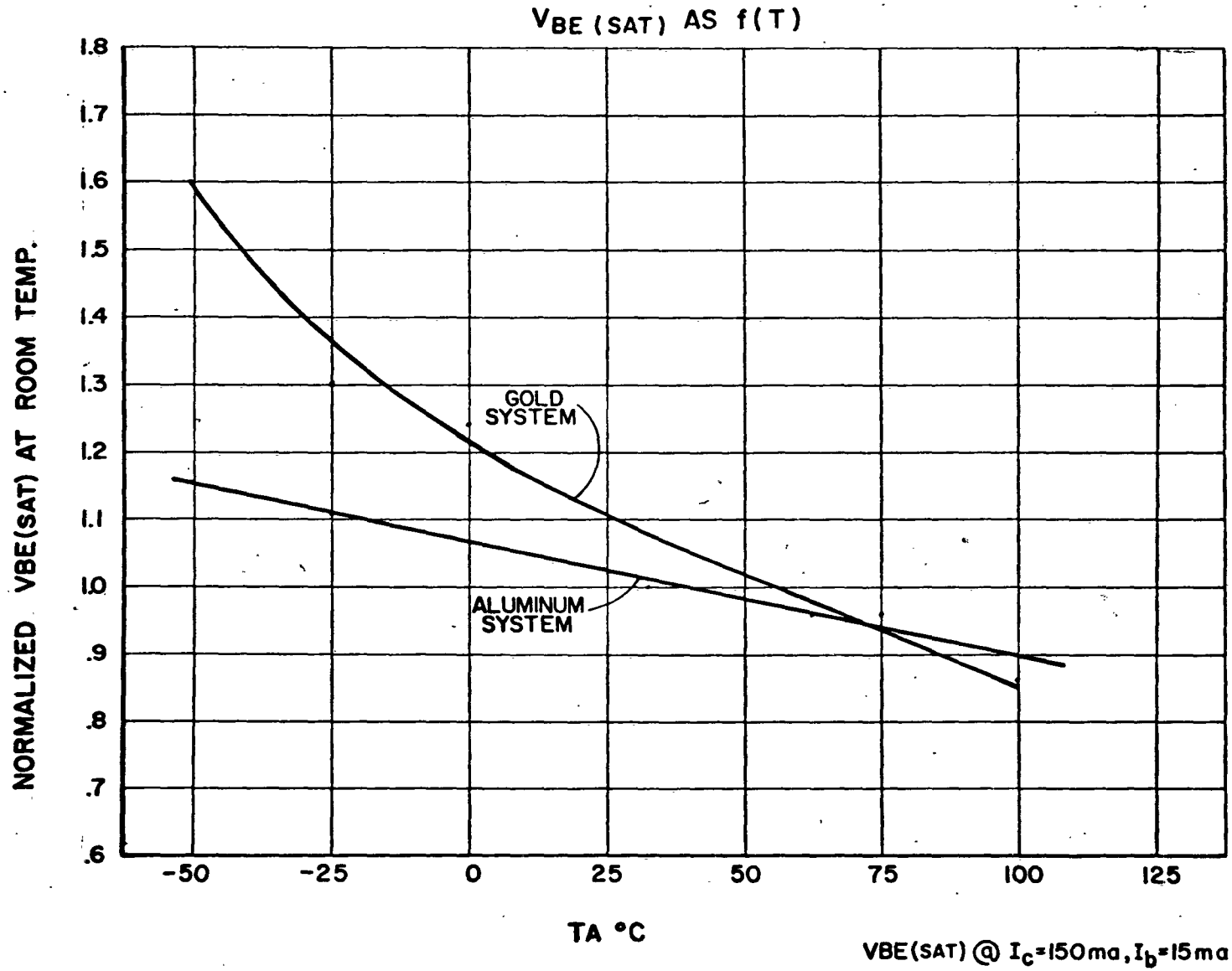

$V_{BE\,(SAT)}$ AS f(T)
NORMALIZED VBE(SAT) AT ROOM TEMP.
1.8
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1.0
.9
.8
.7
.6
GOLD SYSTEM
ALUMINUM SYSTEM
-50
-25
0
25
50
75
100
125
TA °C
VBE(SAT) @ $I_c$=150ma, $I_b$=15ma

FIGURE 2

of temperature and pressure, a process was developed to thermocompression bond the aluminum wire both to the aluminum metalization, and gold plated post. Subsequent aging and mechanical testing showed no significant deterioration of the bonds, even after several thousand hours at 300° C.

## 3.6 Diffusion Processing (Tom Kearkuff)

The major process improvement has been the conversion of the base diffusion to a boron trichloride process replacing the previously used boron oxide process. The boron trichloride has several obvious advantages when compared to the boron oxide diffusion. The boron trichloride gaseous source eliminates many of the difficulties of the boron oxide solid source process, and increases diffusion uniformity across the wafer, from wafer to wafer within the run, and from run to run. It enables us to run up to several hundred wafers at one time through the base and emitter diffusion cycles. This means that samples taken from a run to measure junction depths and base widths are truly characteristic of the run. It also enables a greater volume of material to be run through the same amount of equipment.

During this period, several wire wound furnaces have been brought into operation. The three zone control assures a flat zone up to 30" with a temperature variation of $\pm$ 0.5 °C. This is the limit of the accuracy of our measuring equipment. We feel that the actual temperature variation is less than this. A conservative estimate is $\pm$ 0.25 °C. These furnaces have assisted considerably in improving the consistency of the product.

The base sheet resistance was lowered to enable narrower base widths to be employed, and to improve beta holdup with current.

Experiments are being made to convert the phosphorus oxide emitter diffusion to phosphorus oxychloride. Initial results suggest that the appropriate emitter sheet resistances can be reproduced by this method, and uniformity and yield will be improved. Phosphorus oxychloride, being a liquid source, is more easily controlled, and the handling is simplified considerably.

## 3.7 Die Bonding (Mike Cassidy)

An alternative system of die bonding was evaluated using gold backing of the die to solder the die to the header. This was found to be a practical method of die soldering from a mechanical viewpoint, but electrically, higher $V_{ce(sat)}$ was observed. The use of antimony and arsenic doped gold backing enabled $V_{ce(sat)}$ to be brought down to a lower level; however, the mechanical adherence of the die to the header deteriorated with the addition of the doping agents. However, $V_{ce(sat)}$ was typically 25% higher than the regular furnace-bonded material using a gold-antimony germanium preform. Work is continuing in the evaluation of this die bonding technique in an effort to appreciably decrease the exposure time of the die to the high temperatures required in furnace bonding.

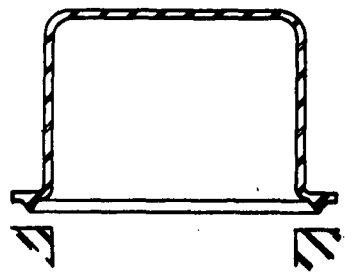
This die bonding technique works well on PNP devices where the gold backing is boron doped.

Up to this time, belt furnace die bonding has been accomplished by the use of a system of jigs and weights. It had been previously felt that the weights were required to ensure adequate wetting between the header, the preform, and the die.

A series of experiments were performed to examine the feasibility of die bonding without the weights, as it was felt that anything resting on the upper surface of the die at elevated temperatures was a possible source of damage or contamination. Without the weights, and using normal procedure, die bonding was possible, but the yields were low. However, it was found that if an ultrasonic vibrator was attached to the belt, die bonding could be accomplished at high yields, and also the appearance of the bond and its mechanical strength improved. The improvement in reliability is intangible, but in general, any process which reduces the possibility of surface contamination should improve the device reliability.

## 3.8 Welding (Mike Cassidy)

With nickel-silver or Kovar cans, problems have been encountered with weld-spatter. This not only gives rise to leakers, necessitating 100% joy bombing, but also causes problems on the final test computer, as the mechanical handling equipment cannot cope with excessive burring. The nickel can with a projection on the bottom lip gives rise to a superior weld which is far more reproducible.



## 4.0 RELIABILITY ENGINEERING (Kenneth W. Davidson)

Work continued on Phase I and Phase II of the Reliability Engineering Program during the quarter.

### 4.1 Encapsulation Experiment

The experiment (hereafter referred to as experiment 1 and experiment 2) to determine an optimum welding process was completed.
The five different welding processes were:

1) $N_2$ Bake (300°C) + $N_2$ Weld (25°C).
2) $N_2$ Purge (25°C) + $N_2$ Weld (25°C).
3) Dry Air Purge (25°C) + Dry Air Weld (25°C).
4) Raw Air Weld (25°C ± 5°C).
5) Activated Moleculer Sieve + Raw Air Weld.

Units which started in the experiments were measured to three specific device type specification limits, as well as to general silicon planar epitaxial transistor specification limits. Figure 1 shows the yields to device types A, B, and C after each environmental test for experiment 1. Using the general limits and considering only catastrophic failures, the yields after each environmental test for experiment 1 are given in Figure 2. The results for the same tests in experiment 2 are given in Figures 5 and 6 respectively. Following the 100% environmental tests, all electrically good units from both experiments and each welding process were divided into two equal groups for life tests. One group of units from each welding process was placed on Operating Life at $V_{CB}$ = 20V and $I_e$ = 40mA and 25°C ambient

temperature. The second group from each welding process was placed on Storage Life at 300°C. Electrical measurements were made initially and at 125, 500, and 1000 hours. The percent yields, to catastrophic failure limits at each reading time, are given for experiment 1 in Figure 3 and for experiment 2 in Figure 7. At the end of 1000 hours of Life Test, a failure rate was calculated for each group and these are given in Figures 4 and 8 respectively.

By ranking the number of occurrences of the various groups, with respect to a given environmental test, and comparing the ranks statistically, the order in which the groups are best is:

| Group | Weld Process |
|---|---|
| 2 | $N_2$ Purge (25°C) + $N_2$ Weld (25°C) |
| 1 | $N_2$ Bake (300°C) + $N_2$ Weld (25°C) |
| 3 | Dry Air Purge (25°C) + Dry Air Weld (25°C) |
| 4 | Raw Air Weld (25°C ± 5°C) |
| 5 | Activated Molecular Sieve + Raw Air Weld |

The life test results from both Operating and Storage, show that the group 2 units perform far superior to those from group 5.

It was concluded from the two experiments that the best welding method for devices fabricated by the gold metalization process is $N_2$ Purge at 25°C plus $N_2$ weld at 25°C.

Additional experiments on later process methods are planned for the next quarter.

## SILICON PLANAR EPITAXIAL TRANSISTOR

### EXPERIMENT 1

### DEVICE YIELDS*

INITIAL READINGS

| GROUP | DEVICE TYPES | | | |
|---|---|---|---|---|
| | A | B | C | TOTAL |
| I | 16.1 | 36.4 | 3.3 | 55.8 |
| II | 17.3 | 40.0 | 3.4 | 60.7 |
| III | 70.5 | 30.3 | 1.7 | 52.5 |
| IV | 20.5 | 28.8 | 6.3 | 54.0 |
| V | 17.4 | 33.0 | 5.8 | 56.2 |

AFTER 60 HR. BAKE

| GROUP | DEVICE TYPES | | | |
|---|---|---|---|---|
| | A | B | C | TOTAL |
| I | 20.3 | 35.6 | 3.3 | 59.2 |
| II | 16.5 | 54.8 | 6.1 | 77.4 |
| III | 17.8 | 40.2 | 5.4 | 63.4 |
| IV | 0.0 | 0.0 | 0.0 | 0 |
| V | 0.0 | 0.0 | 0.0 | 0 |

AFTER ENVIRONMENTAL TESTS

| GROUP | DEVICE TYPES | | | |
|---|---|---|---|---|
| | A | B | C | TOTAL |
| I | 19.5 | 27.1 | 1.7 | 48.3 |
| II | 20.9 | 51.3 | 2.6 | 74.8 |
| III | 18.8 | 36.6 | 6.2 | 61.6 |
| IV | 0.0 | 0.9 | 0.0 | 0.9 |
| V | 0.0 | 0.0 | 0.0 | 0.0 |

*Based on these parameters

(1) BVcbo
(2) BVces
(3) BVebo
(4) Vbe
(5) Vce
(6) ICBO
(7) cob
(8) ft
(9) BVceo
hFE @
(10) 100μA
(11) 1mA
(12) 10mA
(13) 150mA
(14) 500mA

Figure 1

## SILICON PLANAR EPITAXIAL TRANSISTOR

### YIELDS

### EXPERIMENT 1

INITIAL READINGS

| GROUP | INITIAL CATASTROPHIC FAILURES | % YIELDS |
|---|---|---|
| I | 3 | 97.5 |
| II | 1 | 99.1 |
| III | 4 | 96.5 |
| IV | 3 | 97.4 |
| V | 4 | 96.2 |

AFTER 60 HOUR BAKE

| GROUP | CUMULATIVE CATASTROPHIC FAILURES | % YIELDS |
|---|---|---|
| I | 3 | 97.5 |
| II | 1 | 99.1 |
| III | 6 | 94.5 |
| IV | 7 | 93.5 |
| V | 22 | 78.6 |

AFTER ENVIRONMENTAL TESTS

| GROUP | CUMULATIVE CATASTROPHIC FAILURES | % YIELDS |
|---|---|---|
| I | 7 | 94.0 |
| II | 2 | 98.2 |
| III | 18 | 84.0 |
| IV | 53 | 51.8 |
| V | 54 | 47.6 |

FAILURE CRITERIA

| PARAMETER | MIN. | MAX. |
|---|---|---|
| ICBO | - | .5ma |
| hFE (150ma) | 10 | 2000 |

Figure 2

## SILICON PLANAR EPITAXIAL TRANSISTOR

### YIELDS

### EXPERIMENT 1

AFTER 125 HRS.

| GROUP | OPERATING LIFE | | STORAGE LIFE | |
|---|---|---|---|---|
| | INITIAL CATASTROPHIC FAILURES | % YIELDS | INITIAL CATASTROPHIC FAILURES | % YIELDS |
| I | 1 | 98.2 | 2 | 98.2 |
| II | 0 | 100.0 | 0 | 100.0 |
| III | 1 | 97.9 | 17 | 63.0 |
| IV | 4 | 87.1 | 19 | 26.9 |
| V | 11 | 47.6 | 20 | 28.6 |

AFTER 500 HRS.

| GROUP | OPERATING LIFE | | STORAGE LIFE | |
|---|---|---|---|---|
| | CUMULATIVE CATASTROPHIC FAILURES | % YIELDS | CUMULATIVE CATASTROPHIC FAILURES | % YIELDS |
| I | 1 | 98.2 | 2 | 98.2 |
| II | 0 | 100.0 | 0 | 100.0 |
| III | 1 | 97.9 | 19 | 58.7 |
| IV | 5 | 83.9 | 21 | 19.2 |
| V | 11 | 47.6 | 24 | 14.3 |

AFTER 1000 HRS.

| GROUP | OPERATING LIFE | | STORAGE LIFE | |
|---|---|---|---|---|
| | CUMULATIVE CATASTROPHIC FAILURES | % YIELDS | CUMULATIVE CATASTROPHIC FAILURES | % YIELDS |
| I | 1 | 98.2 | 2 | 98.2 |
| II | 0 | 100.0 | 0 | 100.0 |
| III | 2 | 95.8 | 20 | 56.6 |
| IV | 9 | 71.0 | 21 | 19.2 |
| V | 11 | 47.6 | 26 | 7.1 |

CATASTROPHIC FAILURE CRITERIA

| PARAMETER | MIN. | MAX. |
|---|---|---|
| ICBO | - | .5ma |
| hFE (150ma) | 10 | 2000 |

Figure 3

SILICON PLANAR EPITAXIAL TRANSISTOR

EXPERIMENT 1

FAILURE RATE (%/1000 HRS.)

AFTER 1000 HOURS

| GROUP | FAILURE RATE | |
|---|---|---|
| | OPERATING LIFE | STORAGE LIFE |
| I | 4.24 | 5.81 |
| II | 7.27 | 1.98 |
| III | 9.20 | 59.91 |
| IV | 55.45 | 105.66 |
| V | 92.31 | 800.00 |

FAILURE CRITERIA

| PARAMETER | INITIAL | | END POINT LIMITS |
|---|---|---|---|
| | MIN. | MAX. | |
| ICBO | - | 0.1μA | 0.1 μA from initial |
| hFE (150 mA) | 40 | - | 30 min. |

Figure 4

## SILICON PLANAR EPITAXIAL TRANSISTOR

### EXPERIMENT 2

### DEVICE YIELDS*

INITIAL READINGS

| GROUP | DEVICE TYPES | | | |
|---|---|---|---|---|
| | A | B | C | TOTAL |
| I | 6.7 | 25.2 | 0.8 | 32.7 |
| II | 4.7 | 28.5 | 1.5 | 34.7 |
| III | 4.5 | 11.3 | 0.0 | 15.8 |
| IV | 8.5 | 23.4 | 0.0 | 31.9 |
| V | 7.4 | 14.8 | 0.0 | 22.2 |

AFTER 60 HR. BAKE

| GROUP | DEVICE TYPES | | | |
|---|---|---|---|---|
| | A | B | C | TOTAL |
| I | 13.4 | 22.7 | 1.7 | 37.8 |
| II | 12.7 | 32.5 | 2.4 | 47.6 |
| III | 6.8 | 44.2 | 6.8 | 57.8 |
| IV | 17.0 | 46.8 | 0.0 | 63.8 |
| V | 8.6 | 40.7 | 3.7 | 53.0 |

AFTER ENVIRONMENTAL TESTS

| GROUP | DEVICE TYPES | | | |
|---|---|---|---|---|
| | A | B | C | TOTAL |
| I | 12.6 | 24.4 | 1.7 | 38.7 |
| II | 13.5 | 34.1 | 1.6 | 49.2 |
| III | 9.1 | 47.7 | 0.0 | 56.8 |
| IV | 21.3 | 46.8 | 0.0 | 68.1 |
| V | 7.4 | 14.8 | 0.0 | 22.2 |

*Based on these parameters

(1) BVcbo
(2) BVces
(3) BVebo
(4) Vbe
(5) Vce
(6) ICBO
(7) cob
(8) ft
(9) BVceo
hFE @
(10) 100μA
(11) 1mA
(12) 10mA
(13) 150mA
(14) 500mA

Figure 5

## SILICON PLANAR EPITAXIAL TRANSISTOR

### YIELDS

### EXPERIMENT 2

INITIAL READINGS

| GROUP | INITIAL CATASTROPHIC FAILURES | % YIELDS |
|---|---|---|
| I | 0 | 100.0 |
| II | 3 | 97.6 |
| III | 1 | 97.6 |
| IV | 0 | 100.0 |
| V | 9 | 88.9 |

AFTER 60 HR. BAKE

| GROUP | CUMULATIVE CATASTROPHIC FAILURES | % YIELDS |
|---|---|---|
| I | 1 | 99.2 |
| II | 2 | 98.4 |
| III | 1 | 97.6 |
| IV | 0 | 100.0 |
| V | 10 | 82.6 |

AFTER ENVIRONMENTAL TESTS

| GROUP | CUMULATIVE CATASTROPHIC FAILURES | % YIELDS |
|---|---|---|
| I | 2 | 98.4 |
| II | 4 | 96.8 |
| III | 3 | 93.3 |
| IV | 2 | 95.8 |
| V | 12 | 85.2 |

FAILURE CRITERIA

| PARAMETER | MIN. | MAX. |
|---|---|---|
| ICBO | - | 0.5mA |
| hFE (150mA) | 10 | 2000 |

Figure 6

SILICON PLANAR EPITAXIAL TRANSISTOR

YIELDS

EXPERIMENT 2

AFTER 125 HRS.

| GROUP | OPERATING LIFE | | STORAGE LIFE | |
|---|---|---|---|---|
| | INITIAL CATASTROPHIC FAILURES | % YIELDS | INITIAL CATASTROPHIC FAILURES | % YIELDS |
| I | 1 | 98.3 | 0 | 100.0 |
| II | 0 | 100.0 | 0 | 100.0 |
| III | 0 | 100.0 | 0 | 100.0 |
| IV | 0 | 100.0 | 0 | 100.0 |
| V | 0 | 100.0 | 11 | 67.6 |

AFTER 500 HRS.

| GROUP | OPERATING LIFE | | STORAGE LIFE | |
|---|---|---|---|---|
| | CUMULATIVE CATASTROPHIC FAILURES | % YIELDS | CUMULATIVE CATASTROPHIC FAILURES | % YIELDS |
| I | 1 | 98.3 | 0 | 100.0 |
| II | 0 | 100.0 | 0 | 100.0 |
| III | 0 | 100.0 | 0 | 100.0 |
| IV | 0 | 100.0 | 0 | 100.0 |
| V | 1 | 97.1 | 16 | 52.9 |

AFTER 1000 HRS.

| GROUP | OPERATING LIFE | | STORAGE LIFE | |
|---|---|---|---|---|
| | CUMULATIVE CATASTROPHIC FAILURES | % YIELDS | CUMULATIVE CATASTROPHIC FAILURES | % YIELDS |
| I | 1 | 98.3 | 0 | 100.0 |
| II | 0 | 100.0 | 0 | 100.0 |
| III | 1 | 95.2 | 0 | 100.0 |
| IV | 0 | 100.0 | 0 | 100.0 |
| V | 2 | 94.3 | 16 | 52.9 |

CATASTROPHIC FAILURE CRITERIA

| PARAMETER | MIN. | MAX. |
|---|---|---|
| ICBO | - | 0.5mA |
| hFE (150mA) | 10 | 2000 |

Figure 7

SILICON PLANAR EPITAXIAL TRANSISTOR

EXPERIMENT 2

FAILURE RATE (%/1000 HRS.)

AFTER 1000 HOURS

| GROUP | FAILURE RATE | |
|---|---|---|
| | OPERATING LIFE | STORAGE LIFE |
| I | 6.88 | 4.00 * |
| II | 5.17 | 3.60 * |
| III | 5.00 | 10.20 * |
| IV | 10.10* | 10.19 * |
| V | 166.04 | 154.38 |

FAILURE CRITERIA

| PARAMETER | INITIAL | | END POINT LIMITS |
|---|---|---|---|
| | MIN. | MAX. | |
| ICBO | - | 0.1μA | 0.1μA from initial |
| hFE (150 mA) | 40 | - | 30 min. |

* Upper 90% CONFIDENCE LIMITS FOR 0 REJECTS

Figure 8

## 4.2 Acceleration Factor Experiment

The stress factor experiment described in the previous quarterly report was completed during the reporting period. The experiment incorporated devices fabricated during four different time periods, using various types of contact wires for internal connections. The test program was conducted using 400 units for each of four groups. Each group contained devices fabricated from a different time period than the next group. Figure 9 shows the different groups and the method of internal connections to be compared. The method of testing the devices is also shown in Figure 9. In addition to the standard temperature step stress testing, power step stress testing was employed. Two voltage levels were chosen for $V_{CB}$ and the power level was increased in 50mW steps from the maximum 25°C rating of 800mW. Each group of units was measured initially and then subjected to the first stress level for a period of 5 hours. All units were then removed from test for a minimum of 4 hours, and measured again. The cumulative failure distribution for each voltage level was converted to a percentile chart, and the points were plotted as probability on the abscissa versus 1/T as a linear scale on the ordinate. For the power levels, a value of 1/T was determined by converting the power dissipated in the devices to an equivalent junction temperature. A derating factor of 4.57mW/°C was used. After the percentile points for each value of 1/T were calculated, a computer program was written for linear regression analysis. The line of regression which described the points was calculated and drawn on each of the individual plots. In most of the plots, where it was obvious that two failure modes existed, two lines of regression were computed and plotted. These data are presented on each of the four groups,

STEP-STRESS PROGRAM
EXPERIMENT DESIGN

| GROUP | SERIAL | TYPE | CONTACT | WIRE | POST | DATE OF FABRICATION |
|---|---|---|---|---|---|---|
| I | 1-400 | SL-2-01 | Al. | Ag. | Au. | Dec. 1961 |
| II | 401-800 | SL-2-02 | Au. | Au. | Au | Prior to Aug. 1962 |
| III | 801-1200 | SL-2-02 | Au. | Au. | Au. | Oct. 1962 |
| IV | 1201-1600 | AL-2-02 | Au. | Au. | Au. | New Process |

| TYPE OF TEST | TEST CONDITIONS | UNITS | END OF TEST |
|---|---|---|---|
| Power Step Stress | $V_{CB}$=5Vdc start @ 800mw 50mw/step-5 hrs/step-min. off time= 4 hrs. | 1-100, 401-500 801-900, 1201-1300 | @ 63% fail |
| Power Step Stress | $V_{CB}$=40Vdc - other conditions same as above | 101-200,501-600 901-1000,1301-1400 | @ 63% fail |
| Temp. Step Stress | Start Stress @ 200°C Increase by 25°C/Step | 201-300,601-700 1001-1100,1401-1500 | @ 100% fail |
| Operating Life | $V_{CB}$=40Vdc 1E=20mA Readouts - 125,500,1000 | 301-400, 701-800 1101-1200,1501-1600 | 1,000 hrs. |

Figure 9

starting with Group I - 40 volts through Group IV - temperature, in Figures 10 through 21 respectively. From the charts it was determined that Group IV was superior to the other three groups. It may be observed that a fewer percent of the devices fail at a higher temperature in Group IV than in any of the devices in the other groups. This is true for both voltage levels, as well as the temperature test.

To substantiate the conclusion drawn from the step-stress data that the units made in the most recent time period had the lowest failure rate, further analysis were conducted. The per cent failures versus 1/T plots showed that the reliability became progressively better, with the units from the latest process being the best. To determine what the distributions of the leakage and gain parameters did with increasing stress, cumulative per cent versus gain and leakage plots respectively were made on arithmetic probability paper. For the temperature step-stress data, initial readings versus the post 300°C readings were used and Groups I and IV are compared. The initial readings and the post 1050 mW readings were used for both the 5 volt and 40 volt power step-stress data. For the Operating Life data, the initial readings and the 1000 hour readings were used.

starting with Group I - 40 volts through Group IV - temperature, in Figures 10 through 21 respectively. From the charts it was determined that Group IV was superior to the other three groups. It may be observed that a fewer percent of the devices fail at a higher temperature in Group IV than in any of the devices in the other groups. This is true for both voltage levels, as well as the temperature test.

To substantiate the conclusion drawn from the step-stress data that the units made in the most recent time period had the lowest failure rate, further analysis were conducted. The per cent failures versus 1/T plots showed that the reliability became progressively better, with the units from the latest process being the best. To determine what the distributions of the leakage and gain parameters did with increasing stress, cumulative per cent versus gain and leakage plots respectively were made on arithmetic probability paper. For the temperature step-stress data, initial readings versus the post 300°C readings were used and Groups I and IV are compared. The initial readings and the post 1050 mW readings were used for both the 5 volt and 40 volt power step-stress data. For the Operating Life data, the initial readings and the 1000 hour readings were used.

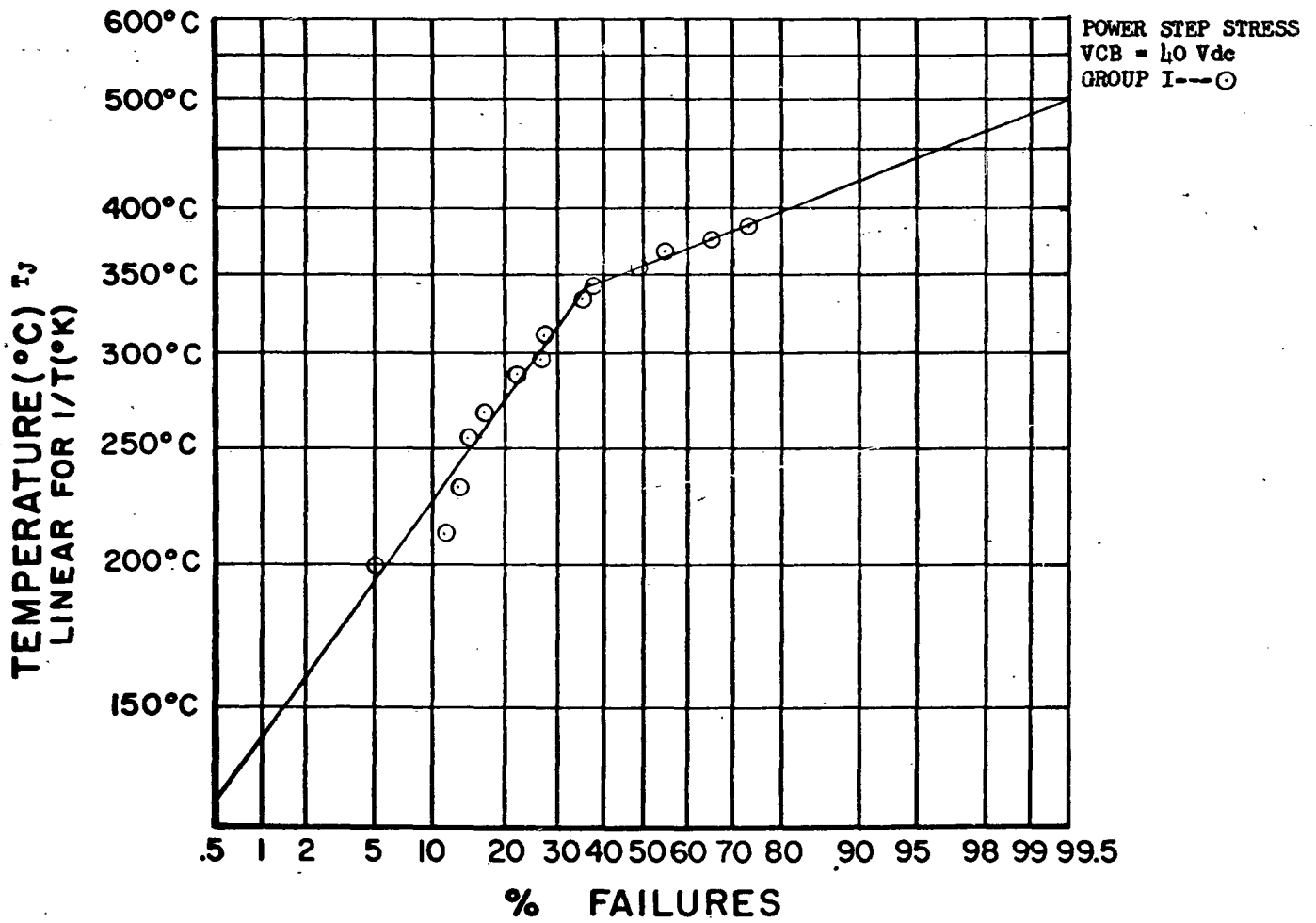

600°C
500°C
400°C
350°C
300°C
250°C
200°C
150°C
TEMPERATURE(°C) Tj
LINEAR FOR 1/T(°K)
.5 1 2 5 10 20 30 40 50 60 70 80 90 95 98 99 99.5
% FAILURES
POWER STEP STRESS
VCB = 40 Vdc
GROUP I---⊙

FIGURE 10

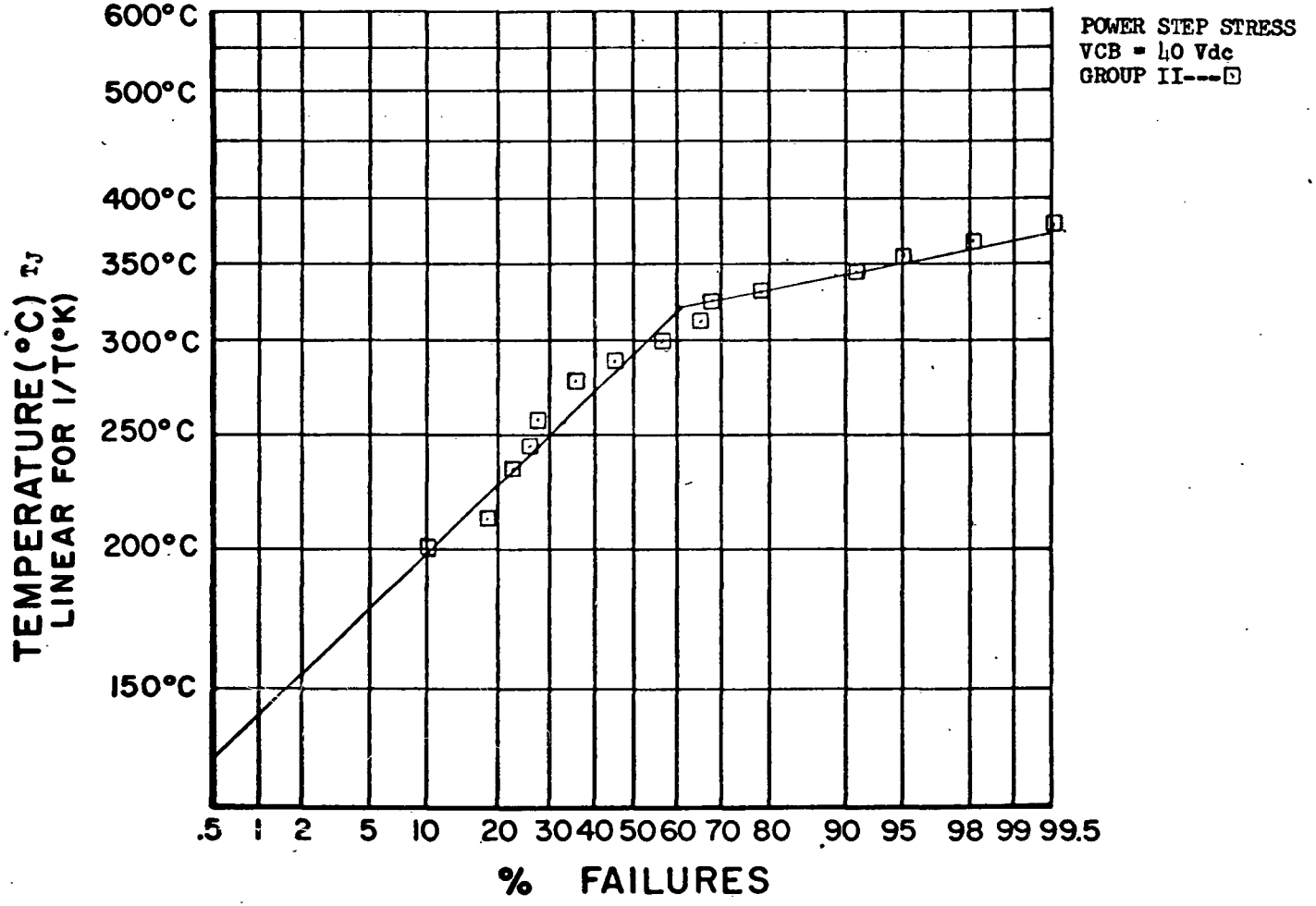

600°C
500°C
400°C
350°C
300°C
250°C
200°C
150°C
TEMPERATURE(°C) $T_J$
LINEAR FOR 1/T(°K)
.5 1 2 5 10 20 30 40 50 60 70 80 90 95 98 99 99.5
% FAILURES
POWER STEP STRESS
VCB = 40 Vdc
GROUP II---⊡

FIGURE 11

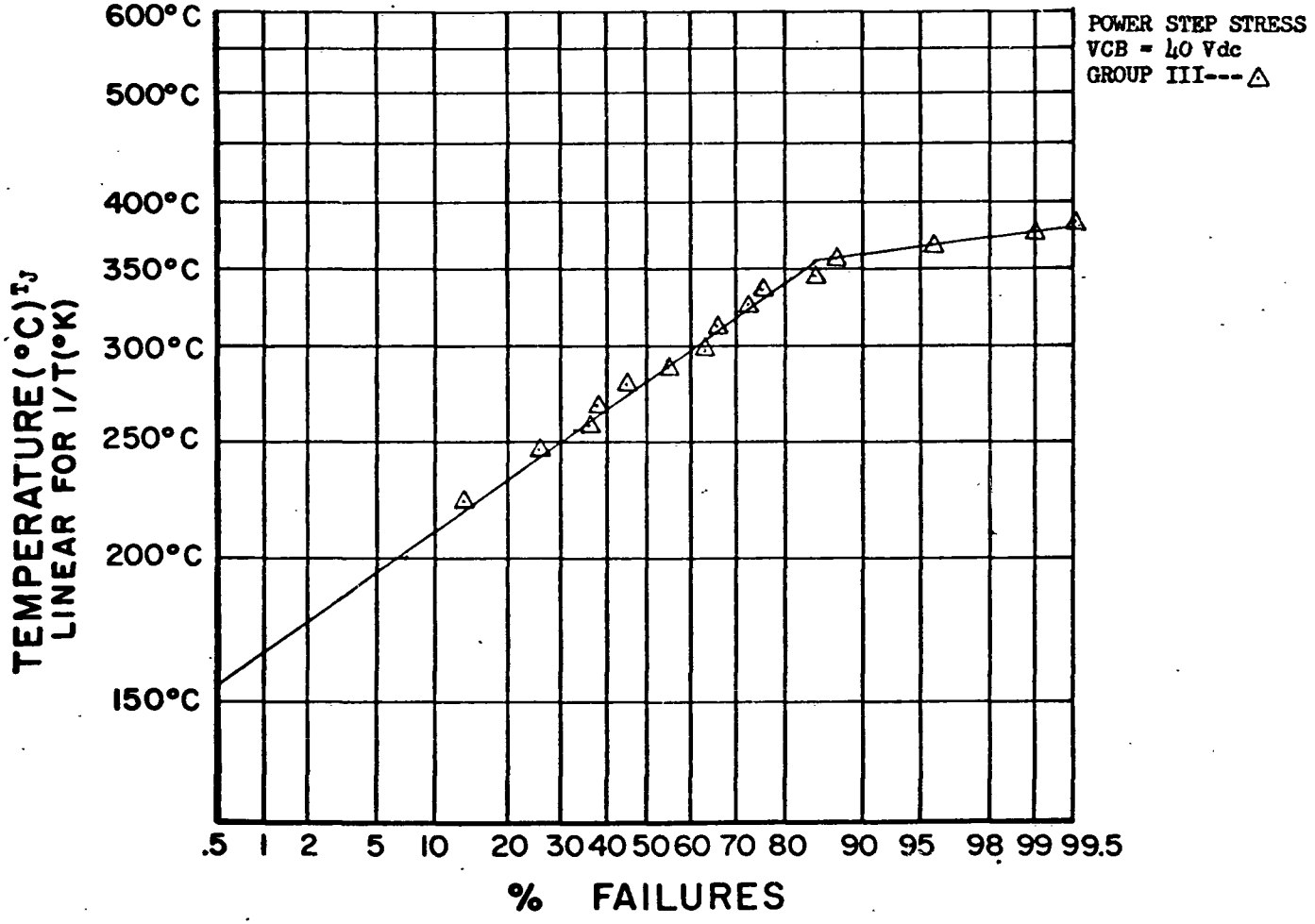

600°C
500°C
400°C
350°C
300°C
250°C
200°C
150°C
TEMPERATURE(°C) $T_J$
LINEAR FOR 1/T(°K)
.5 1 2 5 10 20 30 40 50 60 70 80 90 95 98 99 99.5
% FAILURES
POWER STEP STRESS
VCB = 40 Vdc
GROUP III---△

FIGURE 12

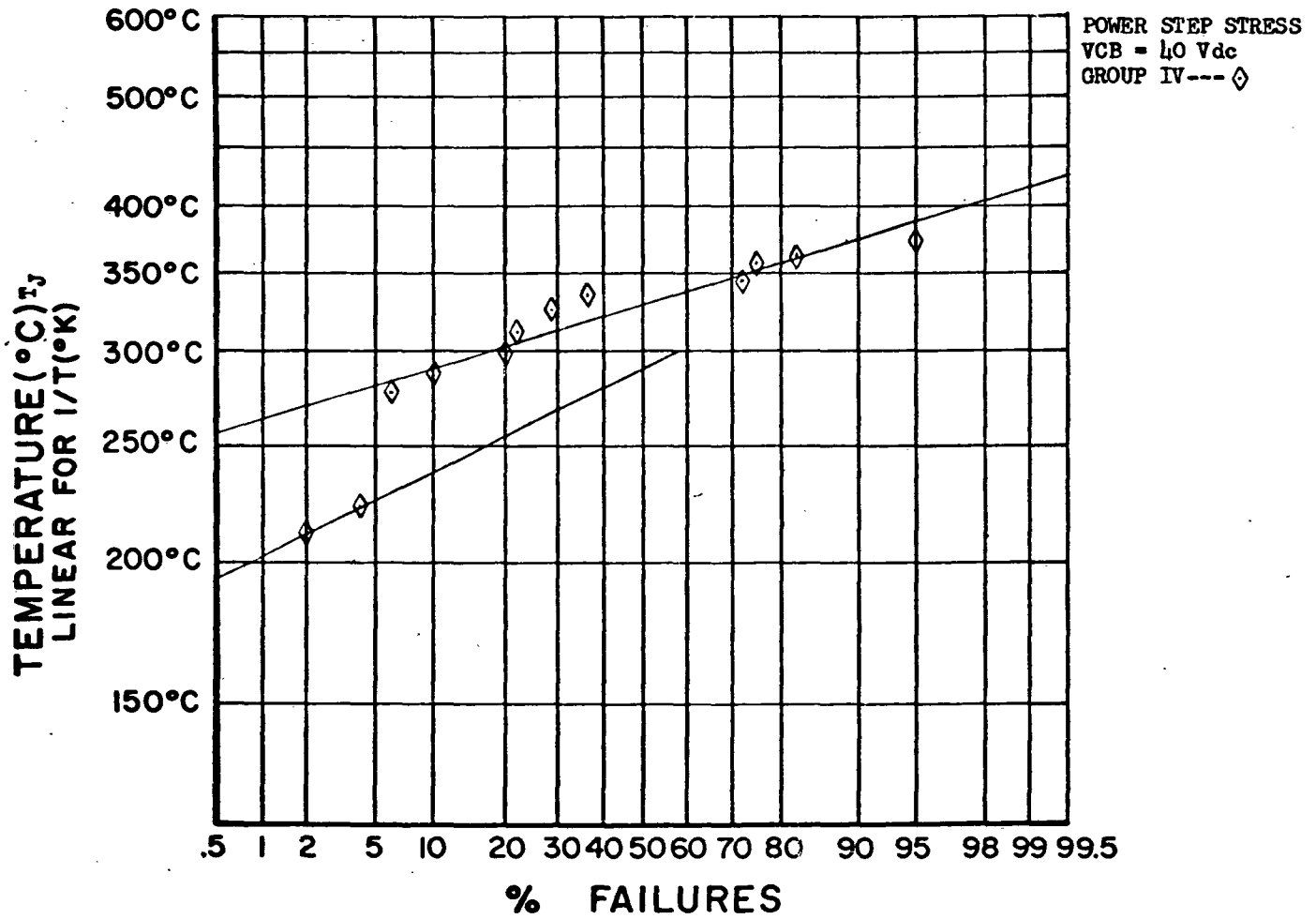

600°C
500°C
400°C
350°C
300°C
250°C
200°C
150°C
TEMPERATURE(°C)$T_J$
LINEAR FOR 1/T(°K)
.5 1 2 5 10 20 30 40 50 60 70 80 90 95 98 99 99.5
% FAILURES
POWER STEP STRESS
VCB = 40 Vdc
GROUP IV---◇

FIGURE 13

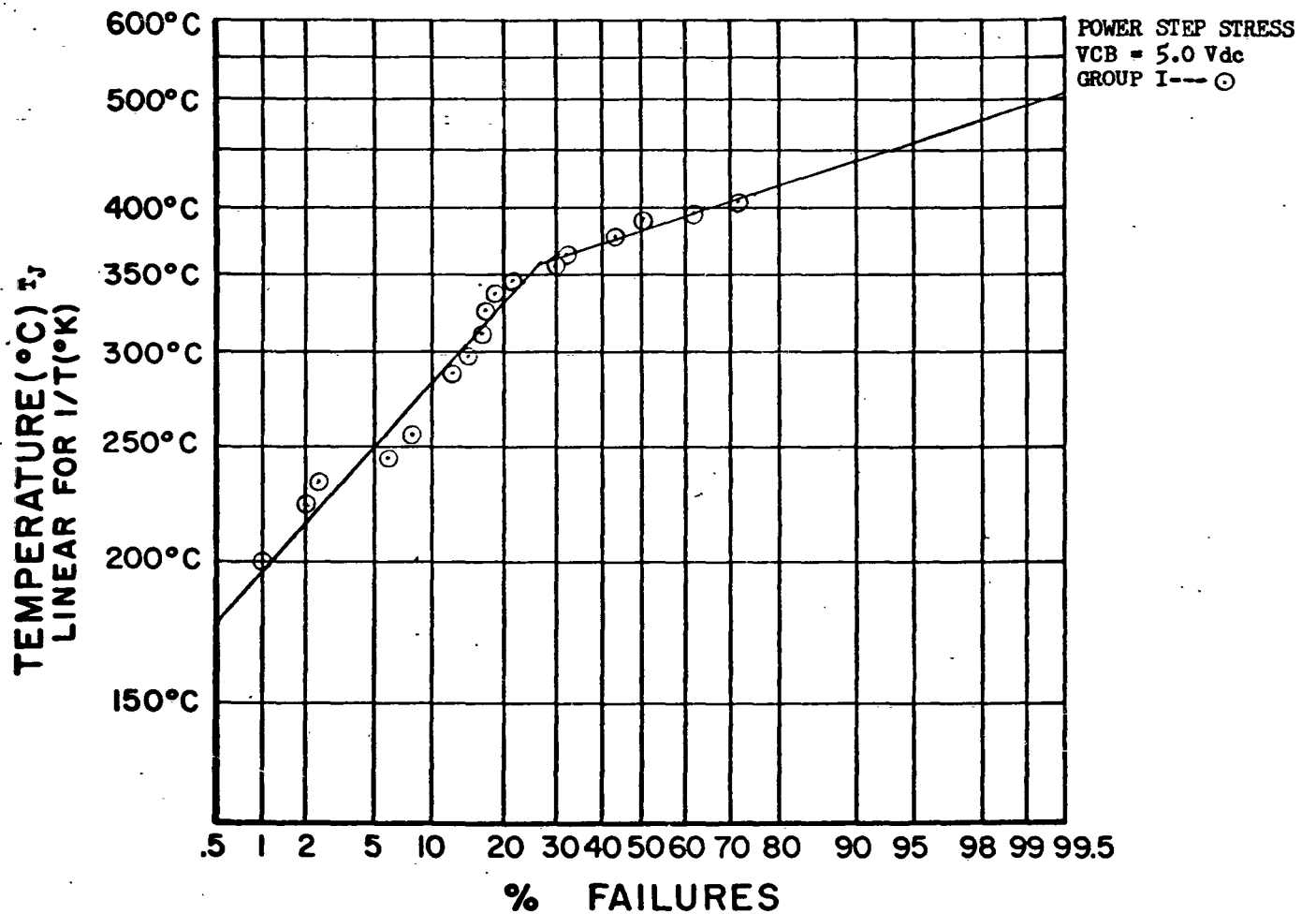

600°C
500°C
400°C
350°C
300°C
250°C
200°C
150°C
TEMPERATURE (°C) $T_J$
LINEAR FOR 1/T(°K)
.5 1 2 5 10 20 30 40 50 60 70 80 90 95 98 99 99.5
% FAILURES
POWER STEP STRESS
VCB = 5.0 Vdc
GROUP I--- ⊙

FIGURE 11

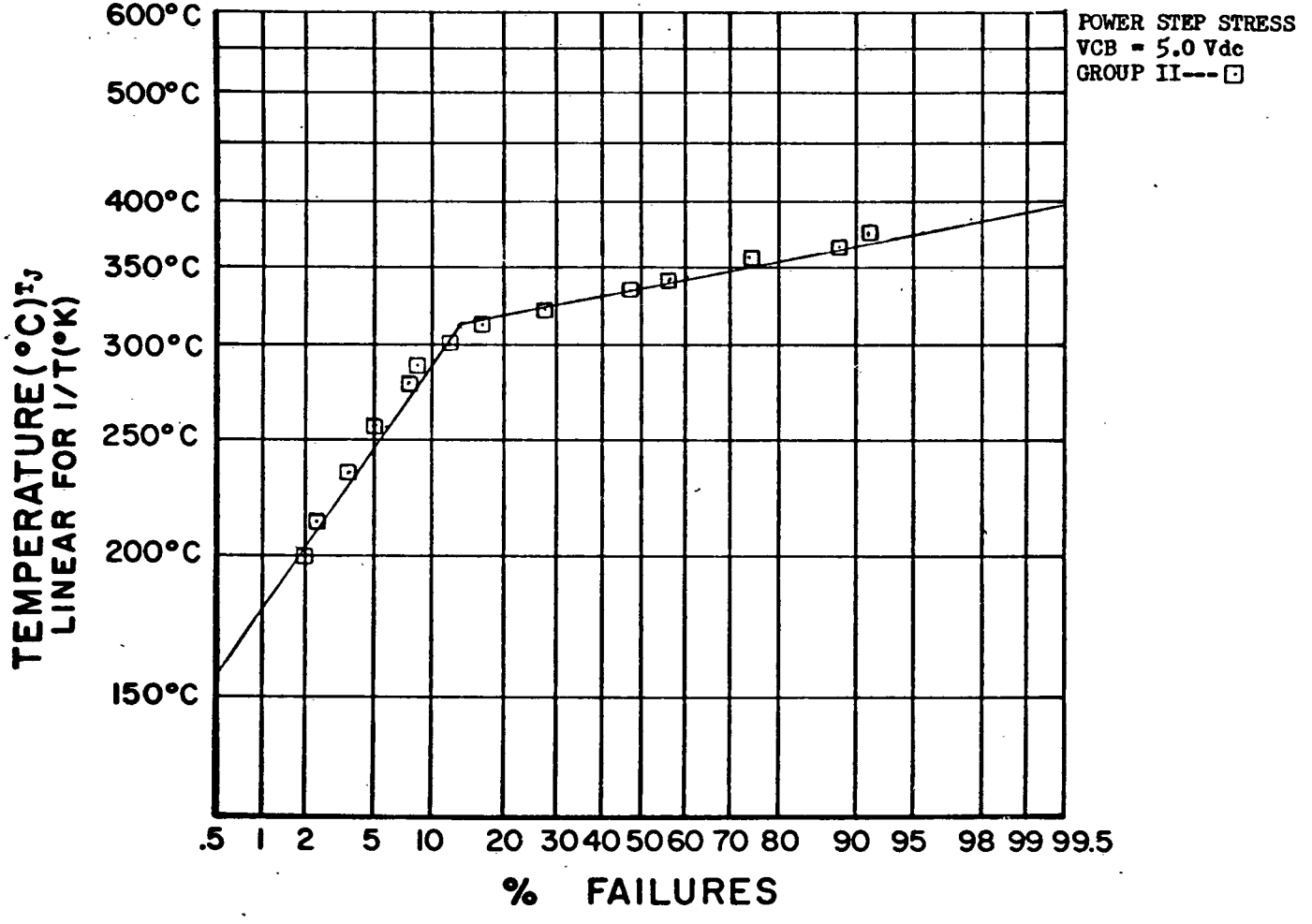

600°C
500°C
400°C
350°C
300°C
250°C
200°C
150°C
TEMPERATURE (°C) $T_J$
LINEAR FOR 1/T(°K)
.5 1 2 5 10 20 30 40 50 60 70 80 90 95 98 99 99.5
% FAILURES
POWER STEP STRESS
VCB = 5.0 Vdc
GROUP II---⊡

FIGURE 15

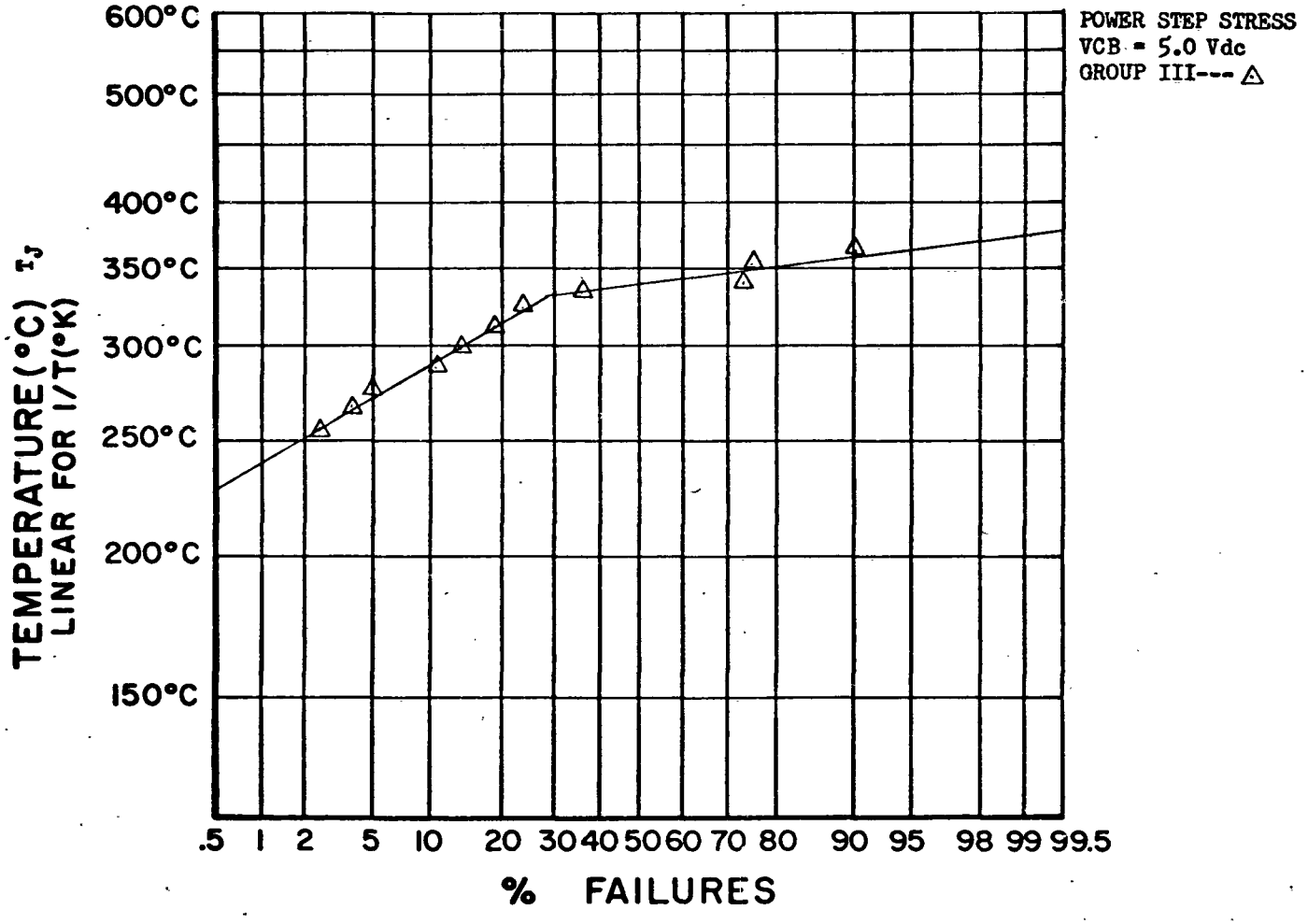

600°C
500°C
400°C
350°C
300°C
250°C
200°C
150°C
TEMPERATURE(°C) $T_J$
LINEAR FOR 1/T(°K)
.5 1 2 5 10 20 30 40 50 60 70 80 90 95 98 99 99.5
% FAILURES
POWER STEP STRESS
VCB = 5.0 Vdc
GROUP III--- △

FIGURE 16

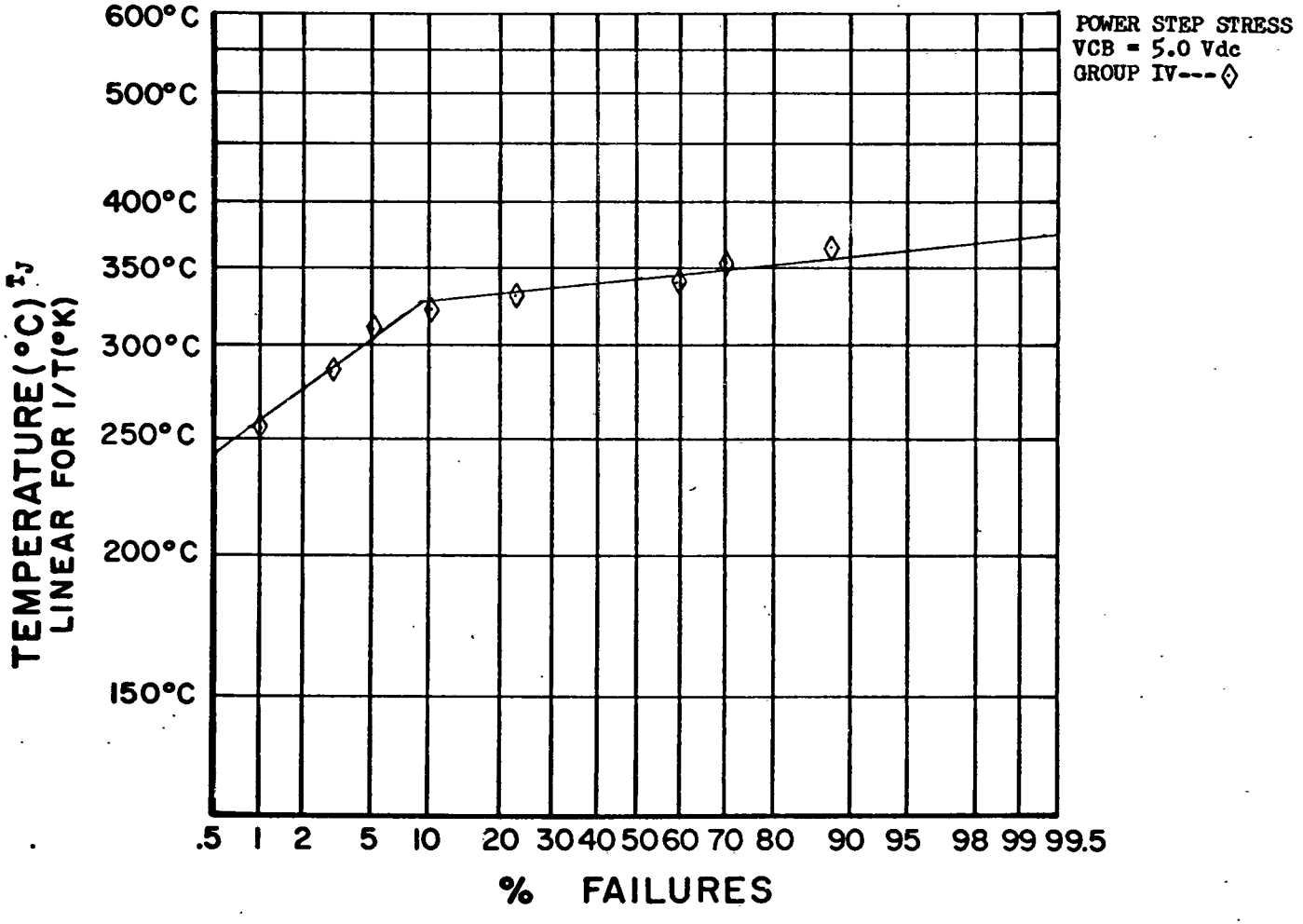

600°C
500°C
400°C
350°C
300°C
250°C
200°C
150°C
TEMPERATURE(°C) $T_J$
LINEAR FOR 1/T(°K)
.5 1 2 5 10 20 30 40 50 60 70 80 90 95 98 99 99.5
% FAILURES
POWER STEP STRESS
VCB = 5.0 Vdc
GROUP IV---◊

FIGURE 17

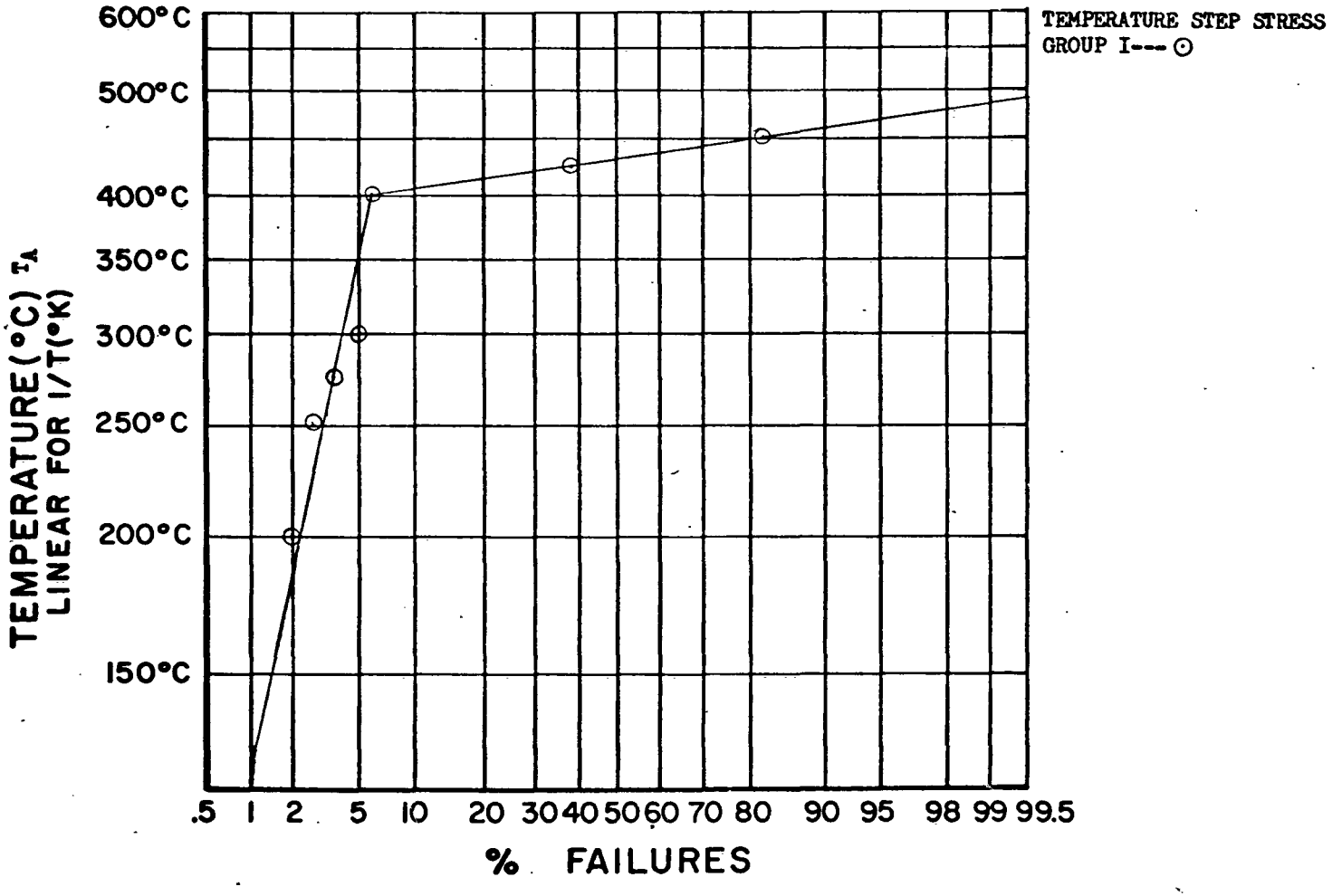

600°C
500°C
400°C
350°C
300°C
250°C
200°C
150°C
TEMPERATURE(°C) $T_A$
LINEAR FOR 1/T(°K)
.5 1 2 5 10 20 30 40 50 60 70 80 90 95 98 99 99.5
% FAILURES
TEMPERATURE STEP STRESS
GROUP I--- ⊙

FIGURE 18

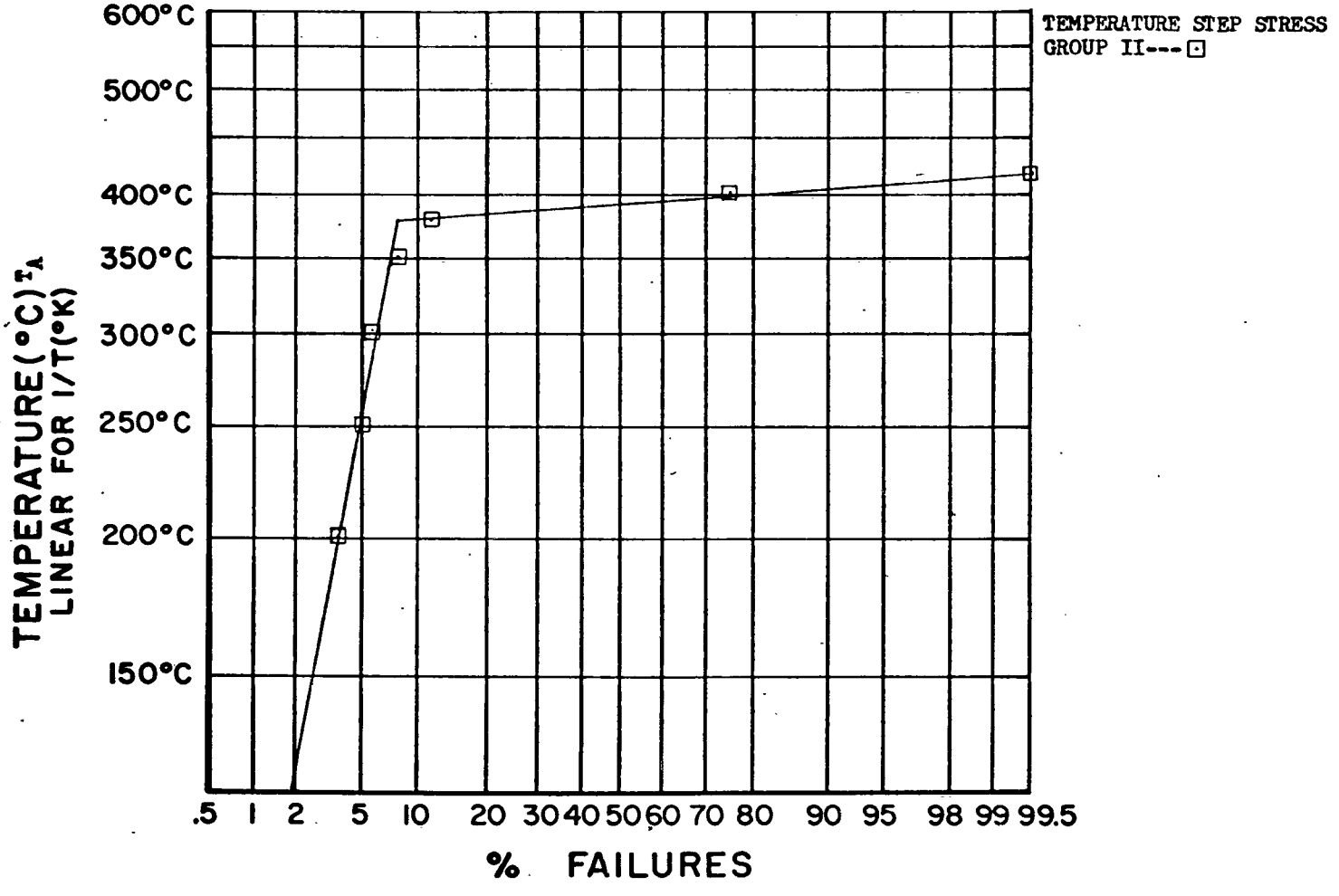

600°C
500°C
400°C
350°C
300°C
250°C
200°C
150°C
TEMPERATURE(°C) $E_A$
LINEAR FOR 1/T(°K)
.5 1 2 5 10 20 30 40 50 60 70 80 90 95 98 99 99.5
% FAILURES
TEMPERATURE STEP STRESS
GROUP II---⊡

FIGURE 19

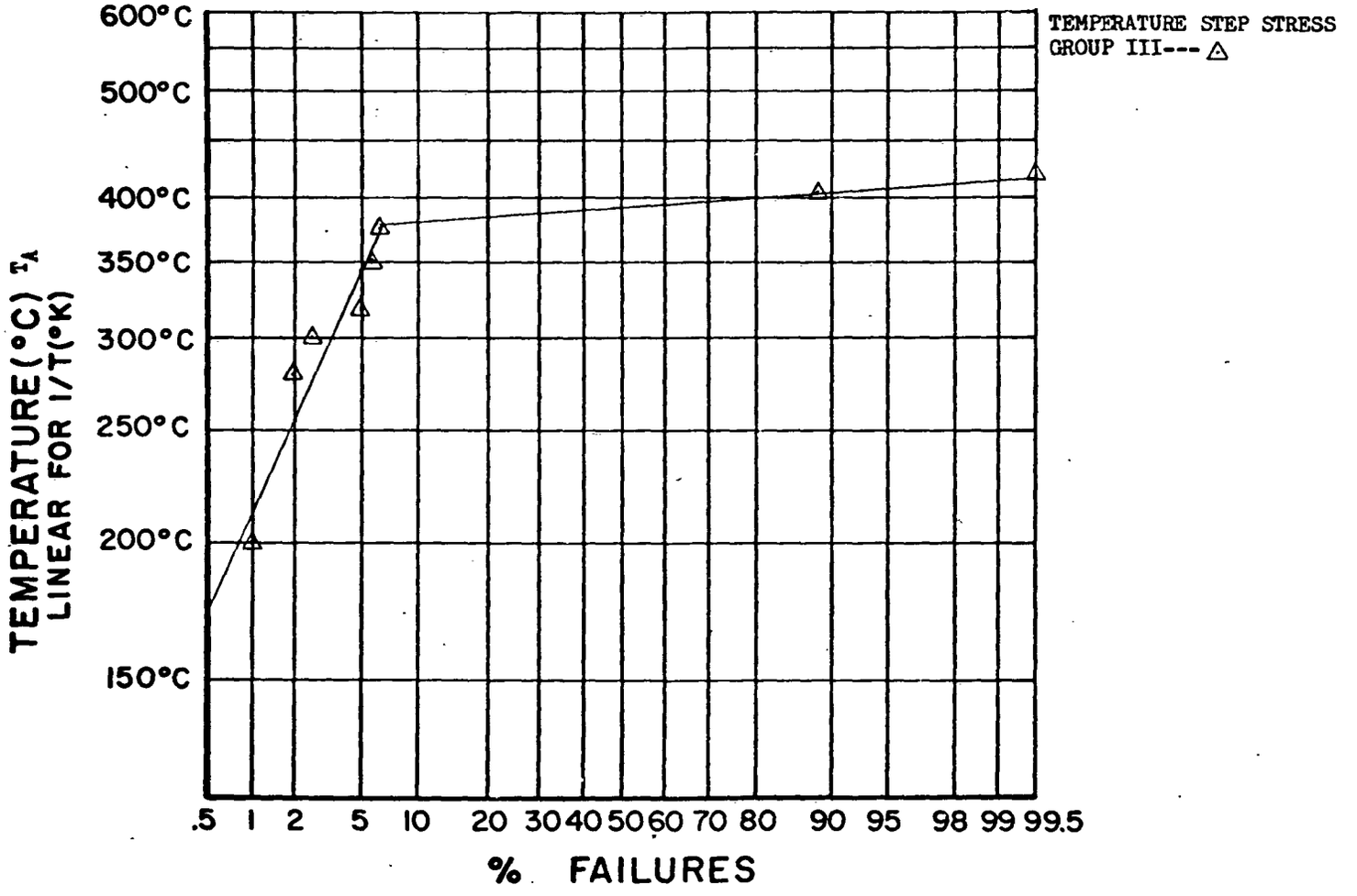

600°C
500°C
400°C
350°C
300°C
250°C
200°C
150°C
TEMPERATURE(°C) $T_A$
LINEAR FOR 1/T(°K)
.5 1 2 5 10 20 30 40 50 60 70 80 90 95 98 99 99.5
% FAILURES
TEMPERATURE STEP STRESS
GROUP III--- △

FIGURE 20

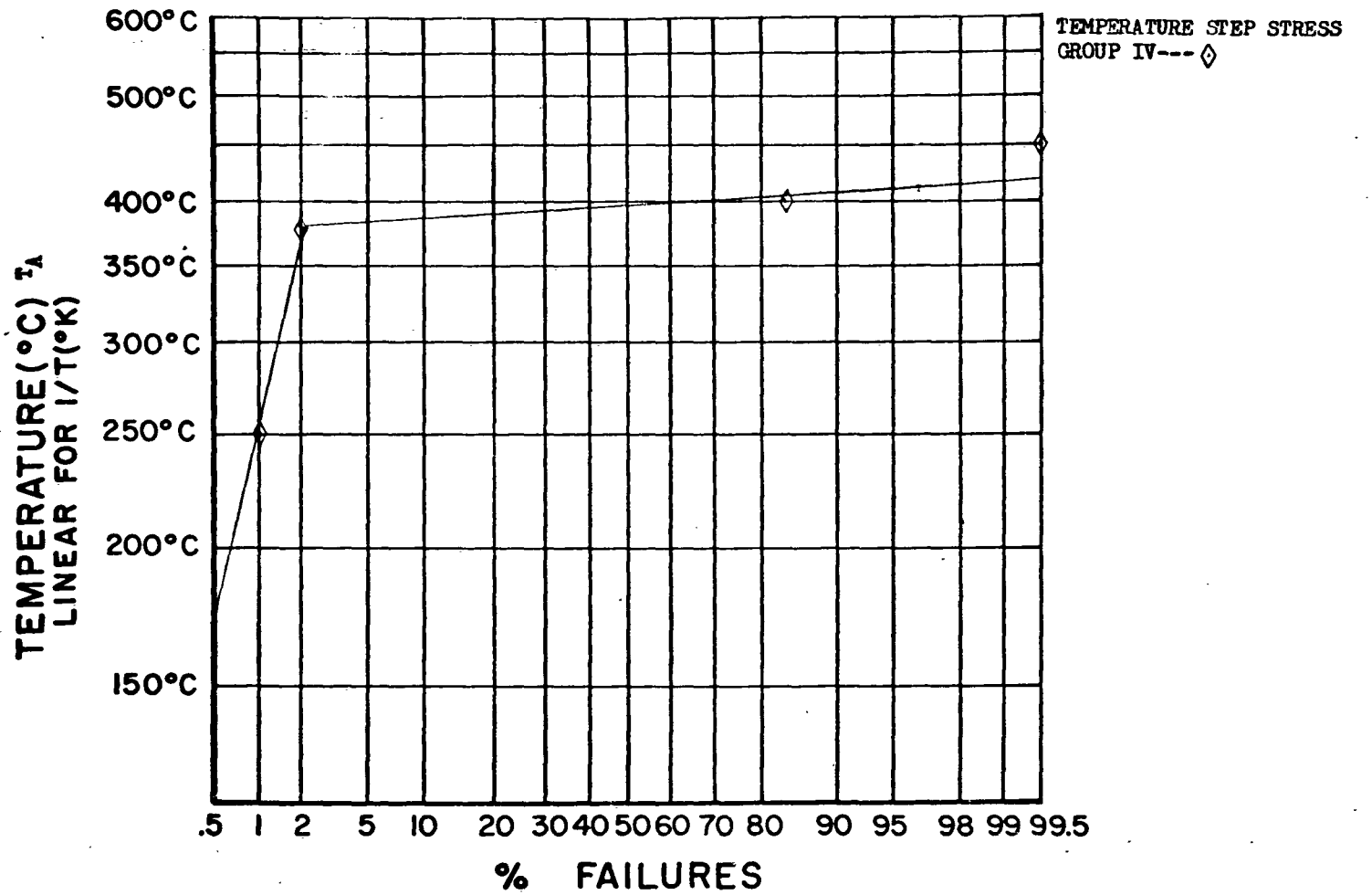

600°C
500°C
400°C
350°C
300°C
250°C
200°C
150°C
TEMPERATURE(°C) $T_A$
LINEAR FOR 1/T(°K)
.5 1 2 5 10 20 30 40 50 60 70 80 90 95 98 99 99.5
% FAILURES
TEMPERATURE STEP STRESS
GROUP IV---◊

FIGURE 21

Figures 22 through 25 show the change in $I_{CBO}$ distributions between Group I and IV. In each of the plots, it is observed that $I_{CBO}$ is more stable in Group IV than in Group I. It is also seen that a larger percent of the distribution shifts by a smaller percentage in Group IV, when compared with Group I in each of the plots.

Figures 26 through 29 show the change in $h_{FE}$ distributions between Groups I and IV. Again the data show that Group IV is far superior to Group I, because $h_{FE}$ is more stable with increasing stress in units from Group IV than in units from Group I.

NO. 3127. ARITHMETIC PROBABILITY. DESIGNED BY HAZEN, WHIPPLE & FULLER
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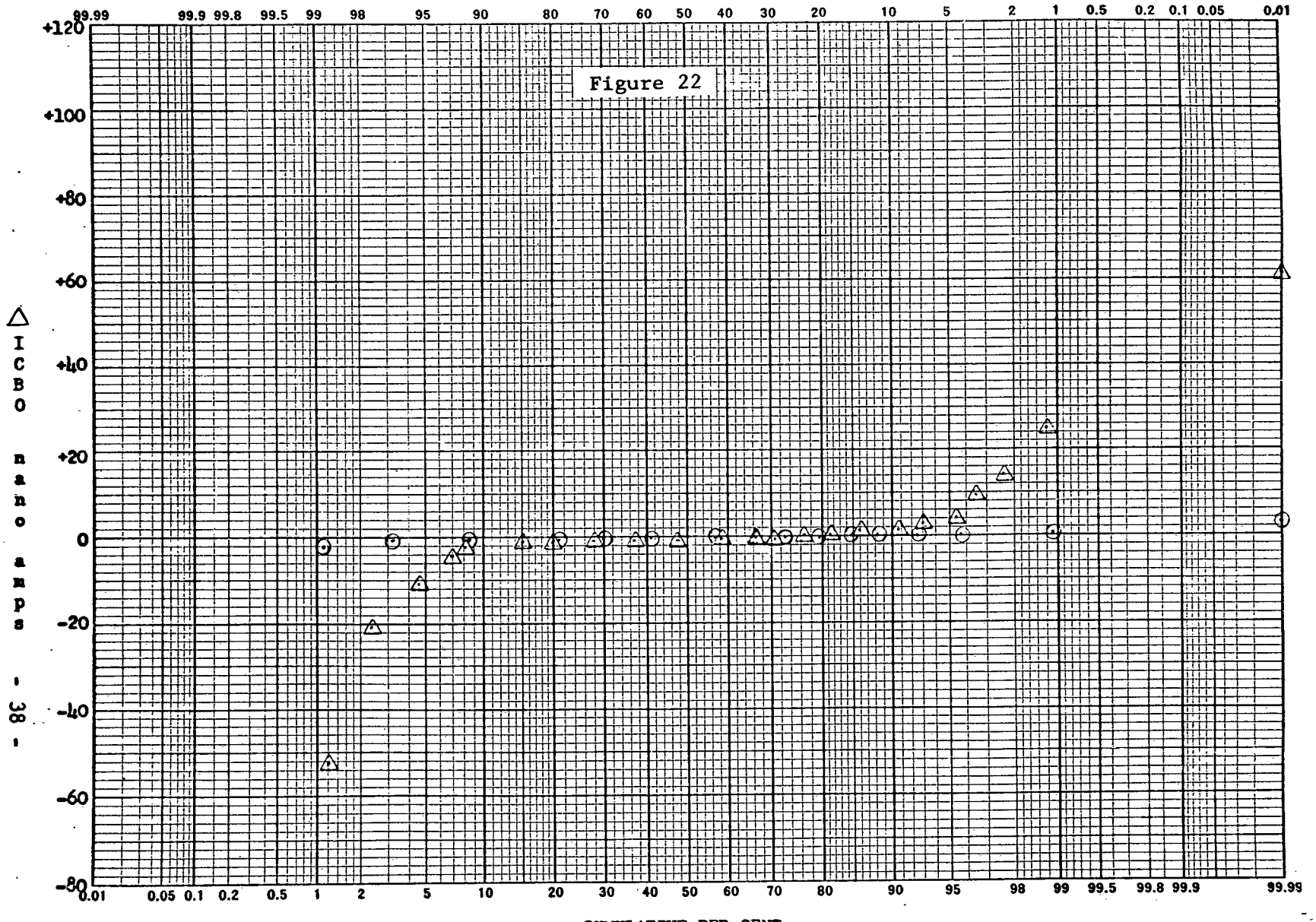
TEMPERATURE STEP STRESS 5 HRS/STEP ΔICBO = (300-0)°C

GROUP I . . . △
GROUP IV . . . ○



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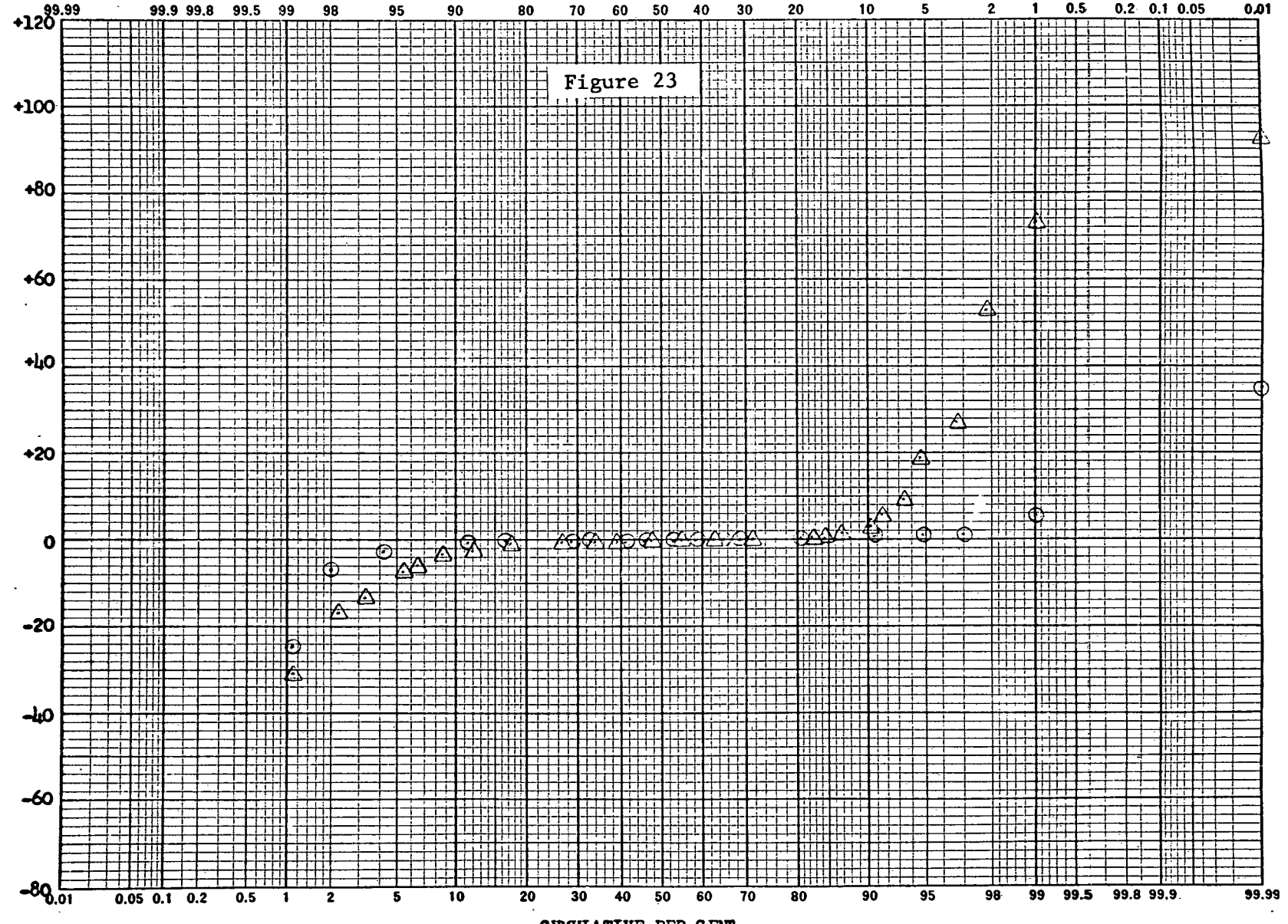
CODEX BOOK COMPANY, INC. NORWOOD, MASSACHUSETTS.

POWER STEP STRESS VCB = 5.0Vdc ΔICBO = (1050-0)mw $T_j$ = 255°C

GROUP I . . . △
GROUP IV . . . ○




Δ I C B O nano amps

CUMULATIVE PER CENT

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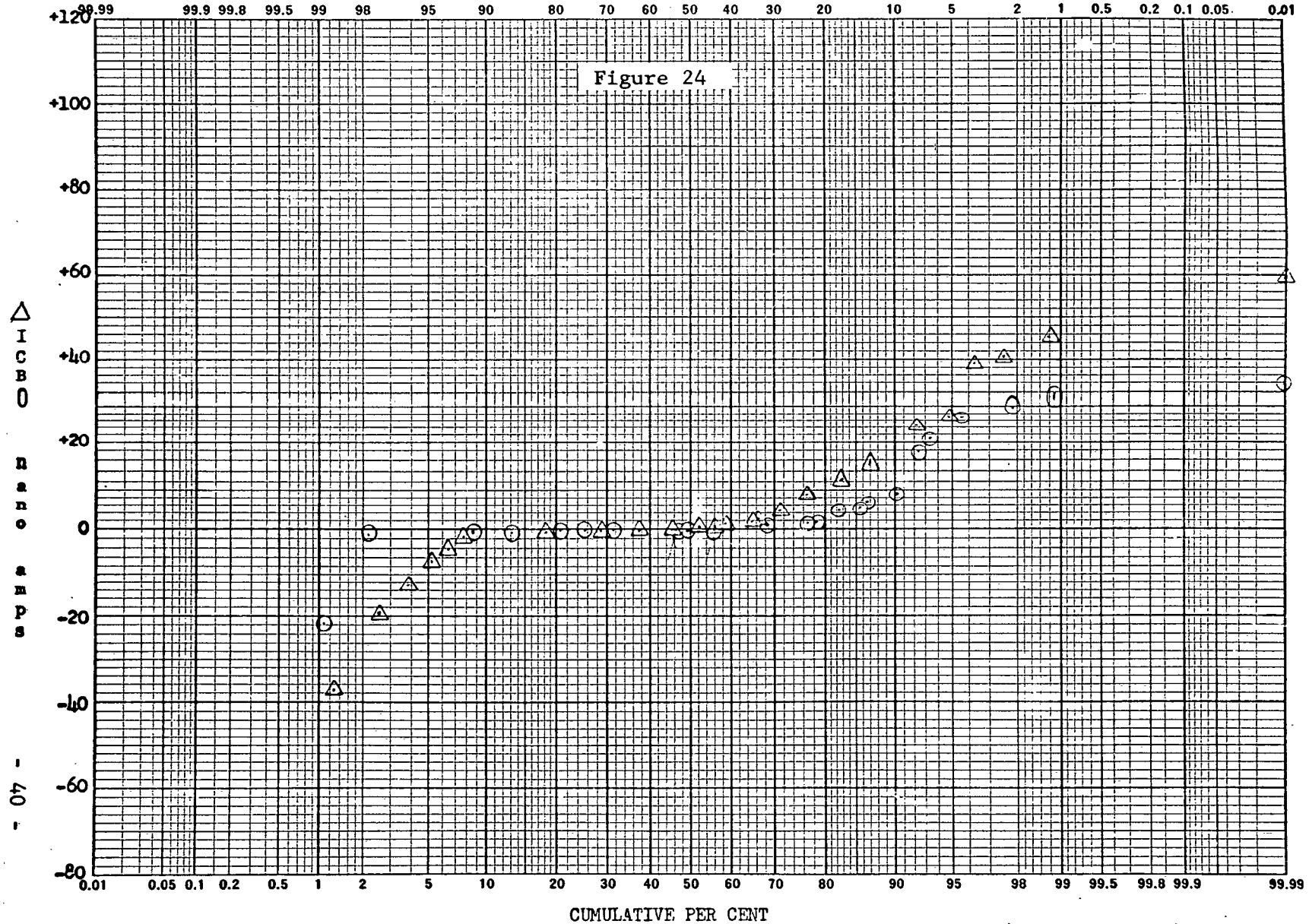
CODEX BOOK COMPANY, INC. NORWOOD, MASSACHUSETTS.

POWER STEP STRESS VCB = 40.0Vdc ΔICBO = (1050-0)mw $T_j$ = 255°C

GROUP I . . . △
GROUP IV . . . ⊙

Figure 24




△ICBO nano amps

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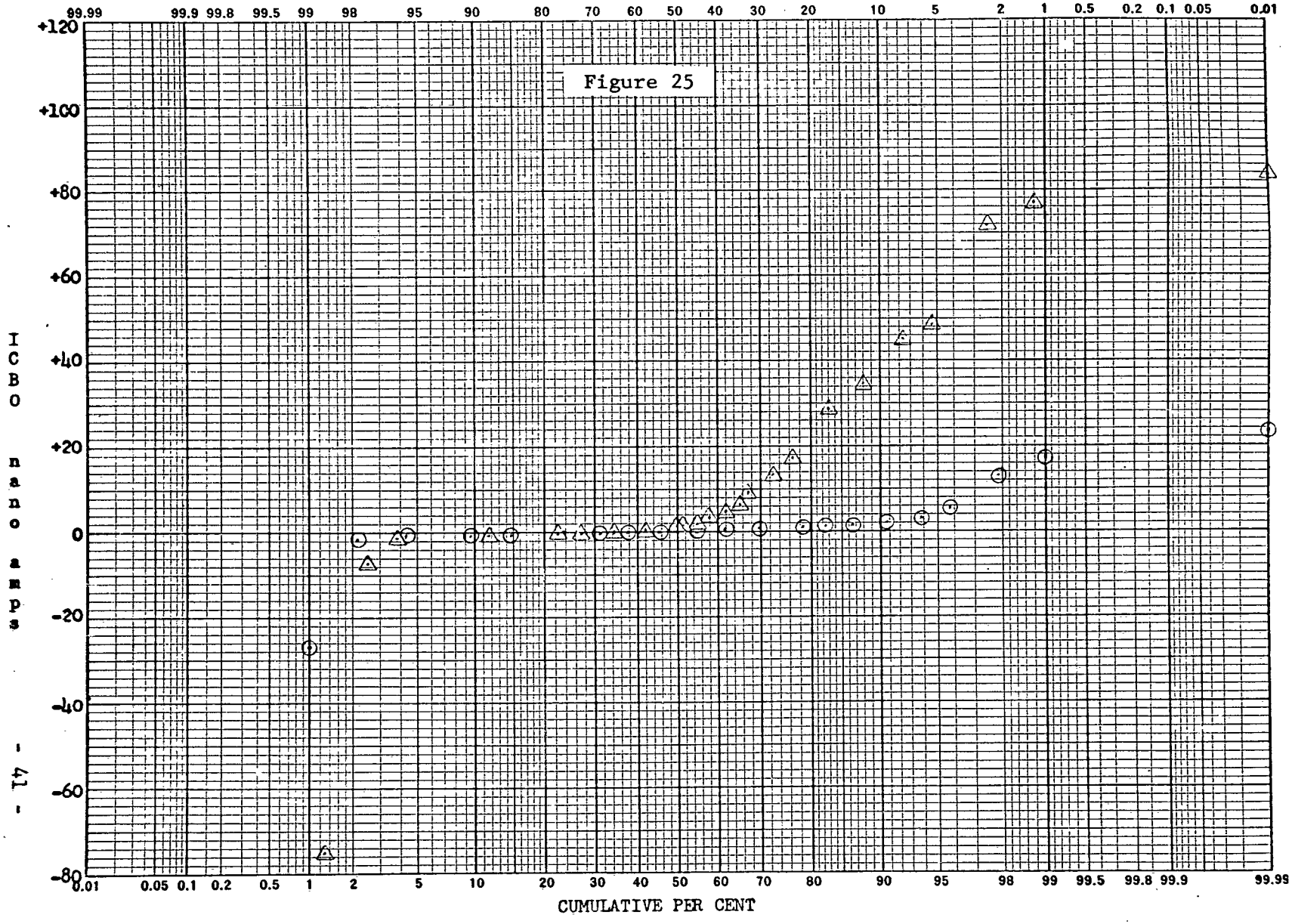
OPERATING LIFE @ VCB = 40Vdc $I_E$ = 20mA $\Delta ICBO$ = (500-0) HRS.

GROUP I . . . △
GROUP IV . . . ⊙

Figure 25



NO. 3127. ARITHMETIC PROBABILITY DESIGNED BY HAZEN, WHIPPLE & FULLER

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TEMPERATURE STEP STRESS 5 HRS/STEP $\Delta hFE = (300-0)^{\circ}C$

GROUP I .... △
GROUP IV .... ⊙

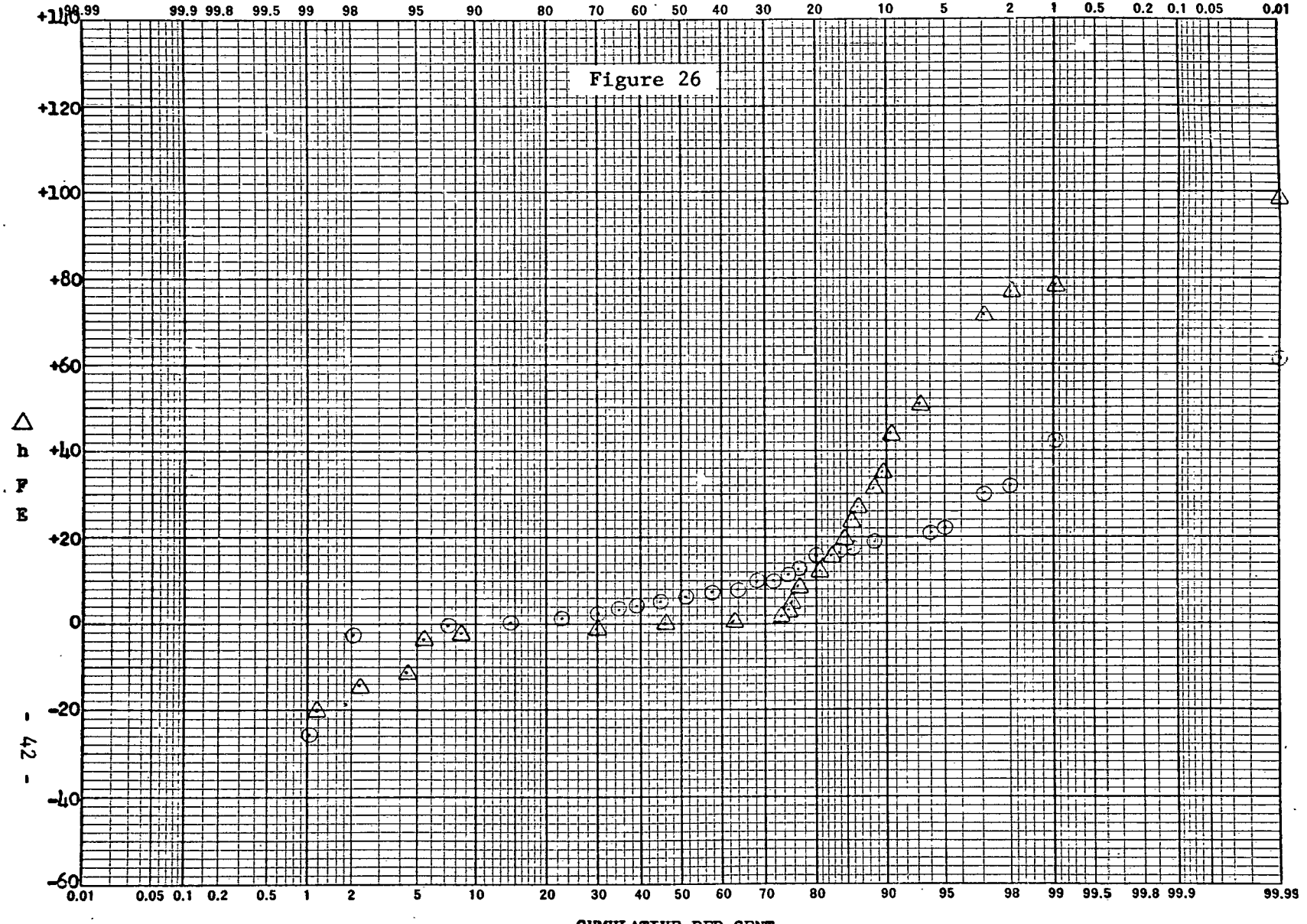


Figure 26

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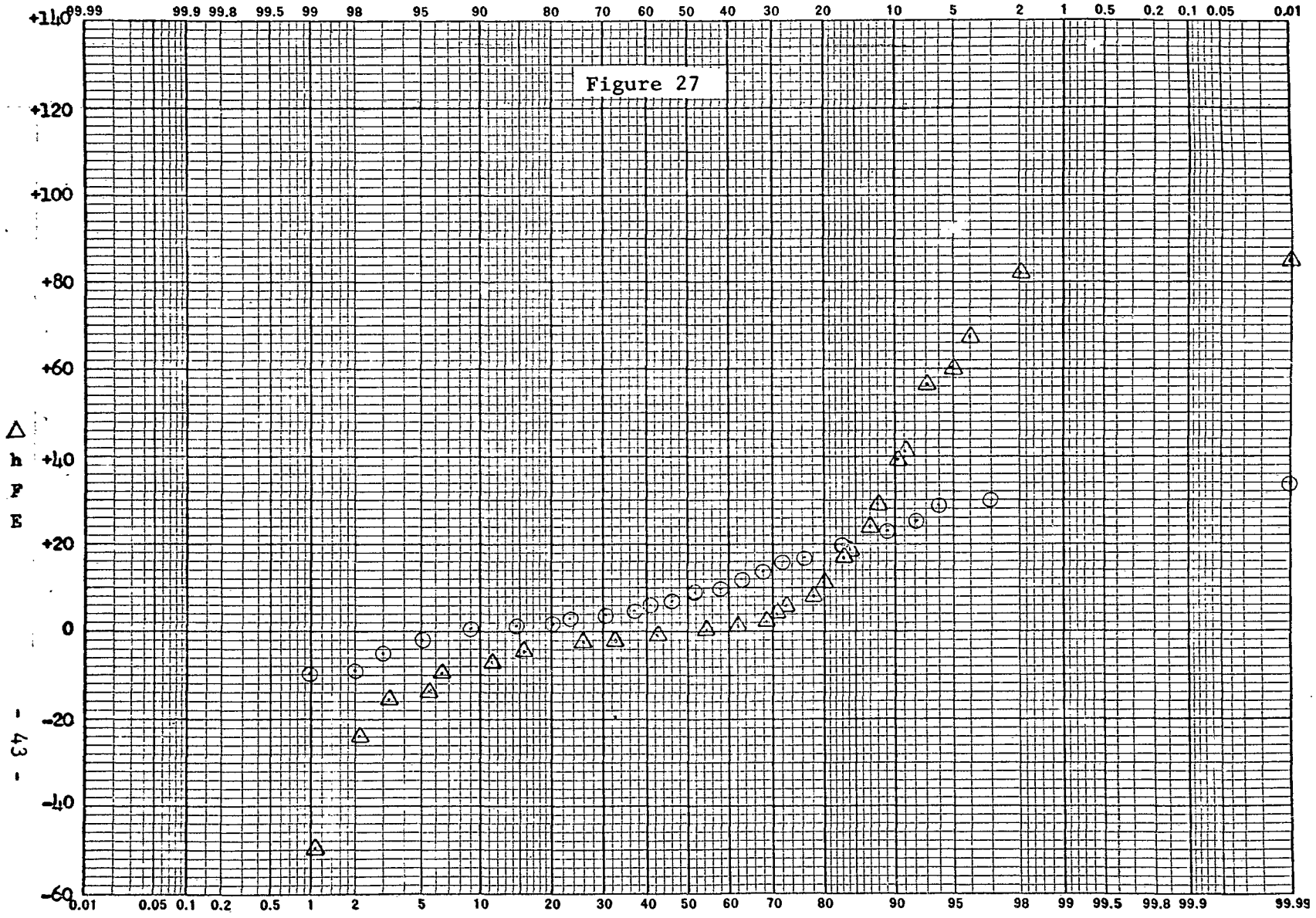
POWER STEP STRESS VCB = 5.0Vdc ΔhFE=(1050-0)mw. $T_j$=255°C

GROUP I....△
GROUP IV....⊙

Figure 27



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POWER STEP STRESS VCB = 40.0Vdc ΔhFE = (1050-0)mw $T_j$ = 255°C

GROUP I . . . △
GROUP IV . . . ○

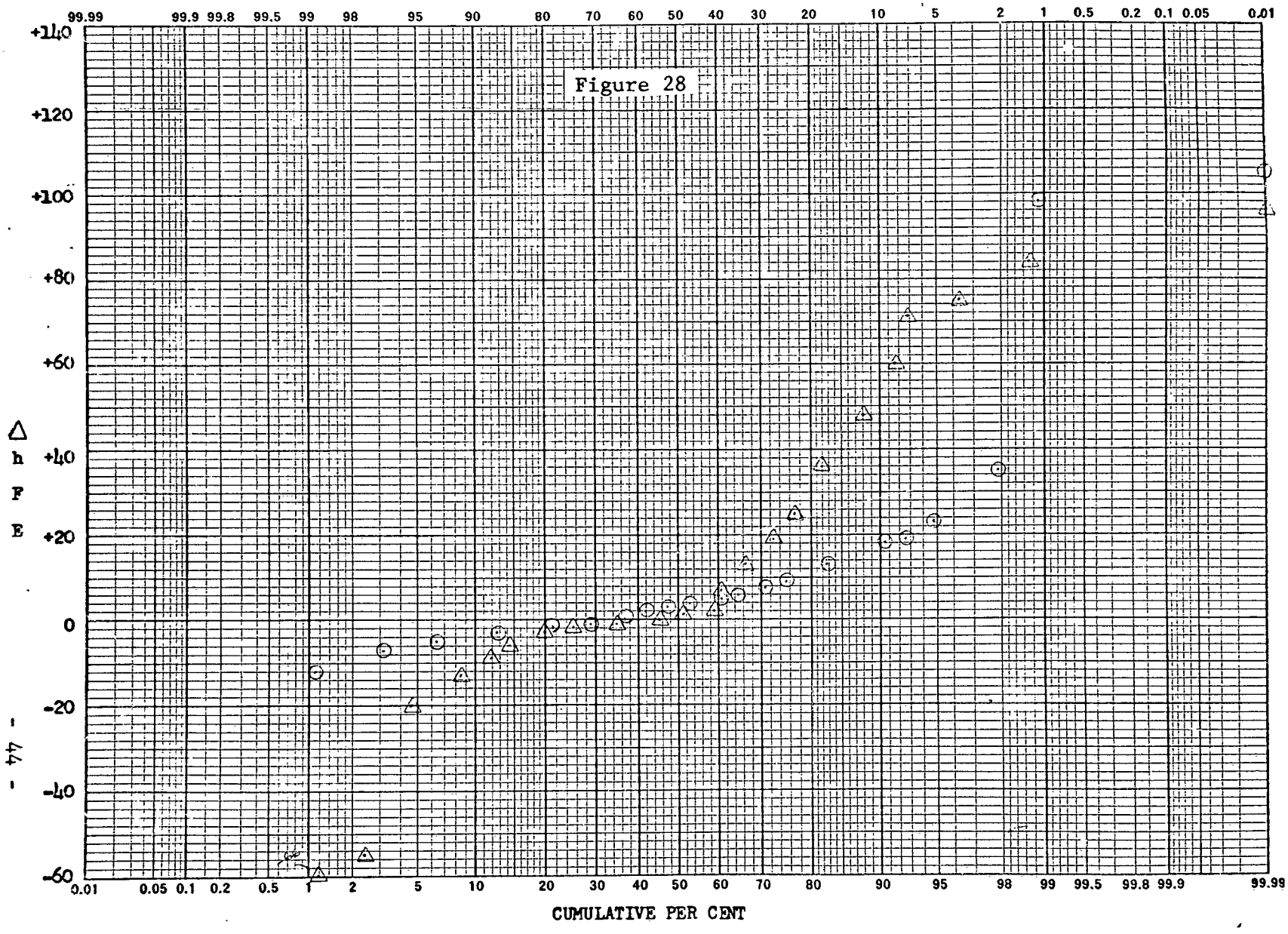


Figure 28

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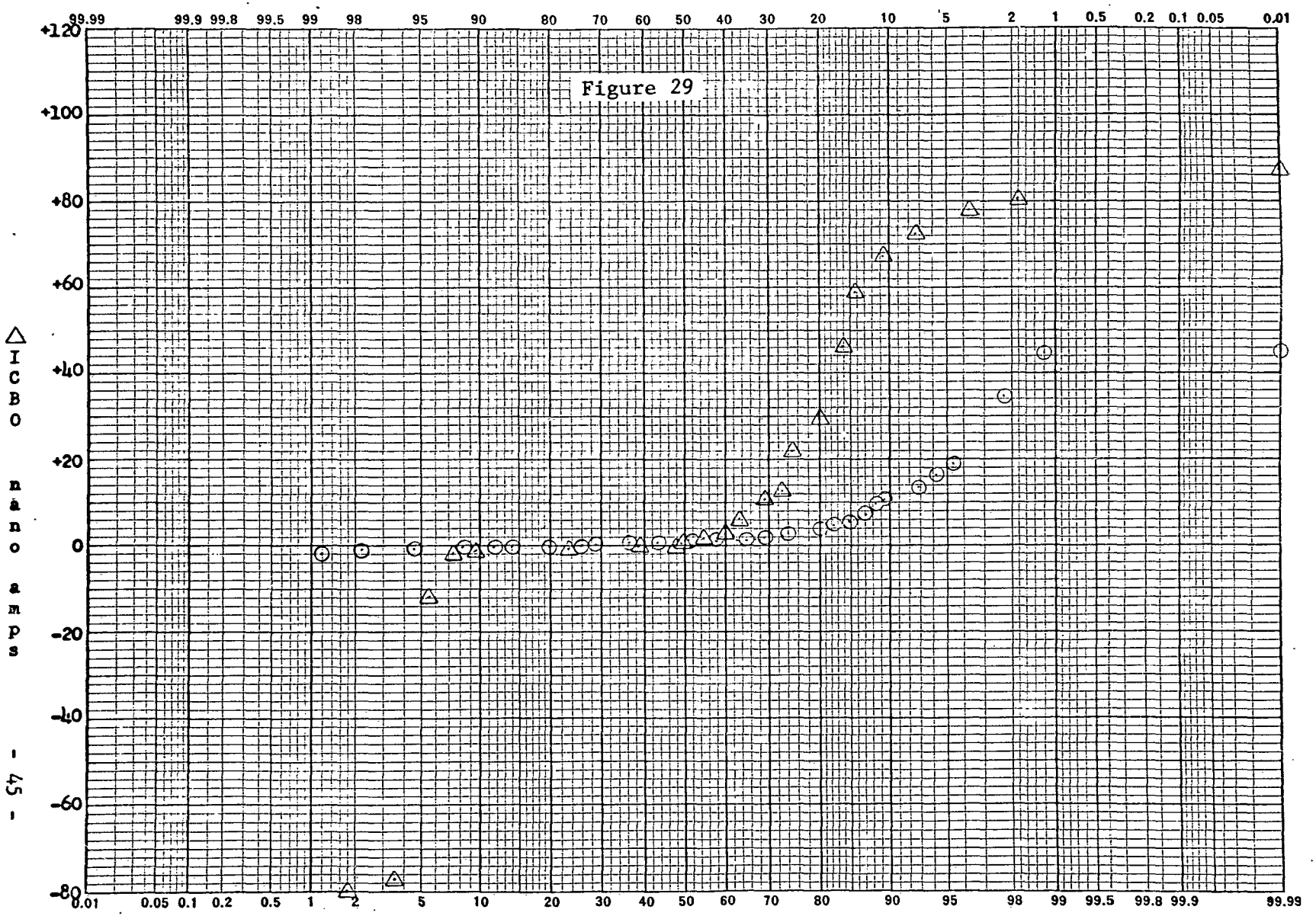
PRINTED IN U.S.A.

OPERATING LIFE @ VCB = 40Vdc $I_E$ = 20mA ΔICBO = (1000-0) HRS. GROUP I . . . △
GROUP IV . . . ⊙

Figure 29



## 5.0 COMPONENT RESEARCH (Byron Mitchell)

Epitaxial passivated silicon NPN wafers with aluminum top-side metalization have been high temperature aged at 500° C for 360 hours in a nitrogen atmosphere. These studies have yielded no evidence of metallurgical degradation for properly aligned patterns; however, at this temperature there is an aluminum oxide formed which, with continued aging with misaligned units, produces failure. These improperly aligned units aged in excess of 360 hours are seen to be shorted-out by the growth of this oxide becoming contiguous with adjacent junctions.

By deleting the gold metalization of the back-side of the wafers, the recognized failure mode of accelerating the solid-state diffusion of this gold-silicon alloy throughout the bulk at this temperature has been effectively indicated and successfully controlled, making possible the protracted investigation of the electrical behavior of these devices. Evaluation of the results obtained by this aging indicates that storage time, as well as high current $\beta$, are shown conclusively to be increased. The collector-to-base diode is degraded. The emitter-to-base diode remains stable.

## 6.0 KEY PERSONNEL

The following key personnel contributed to the contract during the reporting period:

Leo E. Dwork - Manager of Transistor Operations
Wilfred Corrigan - Product Manager, Silicon Devices
Michael Cassidy - Project Engineer, NPN Silicon Line
Wayne Pearson - Engineer, Final Test Evaluation
Henry Rodeen - Engineer
Thomas Kearkuff - Engineering Assistant, Kmer and Diffusion
Kenneth W. Davidson - Manage of Reliability Engineering
Lawrence Cobb - Reliability Engineer, Silicon Products
Carol Pavilack - Mathematician
E. D. Metz - Project Leader, Component Research amd Development Department
Byron Mitchell - Engineer, Component Research and Development Department